Glitch Works 8085 SBC rev 3
GW-8085SBC-3

User's Manual and Assembly Guide

Revision 1, 2018-06-30

Contents

1 Introduction

The Glitch Works 8085 SBC rev 3 (GW-8085SBC-3) is a single-board computer based on the Intel 8085 CPU. It includes the following features:

- Intel 8085 CPU at 2 MHz (guaranteed operation, overclocking possible)
- 64 KB static RAM, FeRAM compatible
- 32 KB ROM, EEPROM, or FeRAM in 4K pages, in-board programmable
- Serial console via Intel 8251A USART
- USART clock independent of system clock
- Software controlled power-on jump
- ROM paging and switch-out
- Debounced reset and power supply supervisory circuit
- Glitchbus expansion header

The 8085 SBC rev 3, when paired with GWMON, is a self-contained system needing only a serial terminal (or teminal emulation software on a PC) for full operation. GWMON for the 8085 SBC rev 3 includes Glitch Works ROM-FS, which allows for the storage of file records in ROM. These records can be loaded from the monitor, or automatically selected by option switches on reset/power-up. This also allows for in-board updates to GWMON without overwriting the current, known-good copy.

2 Configuration

The 8085 SBC rev 3 includes a number of jumpers and switch packs for configuring system options:

Name	Function
J1	ROM Boot, 1-2 disables ROM boot, 2-3 enables ROM boot
J2	ROM Enabled, 1-2 disables ROM on reset, 2-3 enables ROM on reset
J5	Console USART Bitrate, jumper one position only for printed speed
SW2	I/O Port Block Base Address
SW3	ROM Base Address, Write Protect, and Boot Page Address

For normal operation with standard GWMON ROM images, J1 and J2 should both be set 2-3, SW2 should be all open, SW3 1-4 should be closed, and SW3 5-8 should be open. This places the I/O block at `0x00 - 0x03`, ROM at `0xF000 - 0xFFFF`, and enables jump to ROM on reset and power-up.

Console bitrate is selected with J5. The board's silkscreen shows each position's speed. *Only one speed may be selected.* Note that the silkscreen legend will be incorrect if anything other than a 2.4576 MHz crystal is used at Y2.

2.1 Configuring I/O

The addresses of the USART registers, the board status register, and the board control register are controlled by switch pack SW2. In a default configuration, SW2 is set to all open and places the I/O base at `0x00 - 0x03`. The base I/O block may be re-addressed on any four-byte boundary in address space for use with other software.

2.2 ROM Options

ROM configuration on the 8085 SBC rev 3 is flexible. ROM is addressed in 4K pages, using the ROM base set on SW3 and three bits from the board control register. The board control register is software programmable, and is reset to `0x00` at reset and power-on.

A pair of D-type flip-flops allows switching the ROM on or off under software control, as well as mapping ROM to `0x0000` for booting. The default states for these flip-flops are controlled by jumpers J1 and J2. J1 controls remapping to `0x0000` for booting: place its shunt from 1-2 to disable ROM boot, or from 2-3 to enable ROM boot. J2 controls whether the ROM is enabled or disabled at reset. Place its shunt from 1-2 to disable ROM at reset, or from 2-3 to enable ROM at reset. *Note that ROM must be enabled at reset for ROM boot to work (both J1 and J2 must be strapped for 2-3).*

2.3 Interrupt Jumpering

The five hardware interrupt lines of the Intel 8085 are pulled down to an inactive state with 4.7 kΩ resistors. While they are not used by the default Glitch Works software package, they are available for use. Additionally, the `*BINT` line from the Glitchbus expansion header is inverted and brought to TP1, `INTERRUPT`. It may be jumpered to any of the five available hardware interrupts. Consult the schematic for further details.

2.4 Glitchbus Expansion

The 8085 SBC rev 3 is expandable through a Glitchbus expansion header. The Glitchbus is a generic 8-bit bus intended to be processor-agnostic. We plan on offering many expansion boards that utilize this bus design. As implemented on the 8085 SBC rev 3, the Glitchbus is designed to stack above the SBC using PC/104 style stacking headers.

Do note that some of the status and control lines are not fully buffered on the 8085 SBC rev 3 and are subject to loading limitations.

The 8085 SBC's Glitchbus expansion header is not compatible with previous expansion boards designed for past revisions of the Glitch Works 8085 SBC. Previous boards will not work with the 8085 SBC rev 3 – use only Glitchbus compatible expansion boards! Previous boards are of a different physical size and should be fairly hard to get mixed up with Glitchbus boards.

3 Assembly

The 8085 SBC rev 3 is designed to be easy to assemble for anyone with moderate soldering ability. It is a moderately complex board and will typically require between one and three hours of assembly time, depending on the skill of the assembler. The following tools will be required:

- Soldering iron, 20-40 W recommended, grounded tip
- Solder, 63/37 leaded solder recommended, Kester "44 Core" or similar
- Diagonal cutters or flush cutters
- Solder braid, solder sucker, or desoldering station, in the event errors are made
- Needle-nose pilers for bending component leads
- 1/4 and 1/8 W resistor lead forms (optional)

This manual does not cover basic soldering technique. If you are new to soldering, we recommend the Adafruit soldering guide and plenty of practice on a piece of protoboard, before beginning assembly of the 8085 SBC rev 3. The Adafruit guide can be found at:

`https://learn.adafruit.com/adafruit-guide-excellent-soldering`

3.1 Assembling the 8085 SBC rev 3

If you purchased a full Glitch Works parts kit, we recommend completing all assembly sections, since extra features can be disabled as needed. If supplying your own parts, you may choose which sections to complete based on the functionality required.

Note that pin 1 is designated with a square pad for all ICs, resistor packs, switches, and most connectors. Pin 1 is toward the top of the board, as seen from the front, for all ICs, diodes, resistor packs, and switches. The component (front) side of the board is the side which contains the white silkscreen legend. It is recommended to install components from shortest to tallest, which makes assembly without an assembly vise or jig easier, assuming the board is flipped over and soldered with the component side resting on a table top.

All jumper headers and connector headers are press-fit and may require a bit of force or gentle wiggling to install. This is normal and helps keep the headers in place when the board is flipped over for soldering.

3.2 Assembly Checklist

- ☐ Verify parts list against kit contents or builder-provided parts
- ☐ Consult the assembly drawing for component locations and values
- ☐ Bend all 0.01 µF bypass capacitors (yellow axial bead) – position 2 on a 1/8 W lead form
- ☐ Install all 0.01 µF capacitors in positions marked C in assembly diagram
- ☐ Hairpin bend three 4.7 kΩ resistors and set aside
- ☐ Bend remaining 4.7 kΩ resistors and install in their marked locations – position 1 on a 1/4 W lead form
- ☐ Bend all 330 Ω resistors and install in their marked locations – position 1 on a 1/4 W lead form
- ☐ Install non-socketed DIP ICs at their marked locations. Do not install U9, U15, U16, U17, U19, or U21
- ☐ Install a 16-pin socket at U21
- ☐ Install 28-pin sockets at U15, U16, U17, and U19
- ☐ Install a 40-pin socket at U9
- ☐ Install 22 µF 10V capacitors at C8 and C17, bend leads with needle-node pliers
- ☐ Install micro tact pushbutton at SW1
- ☐ Install 20 pF radial ceramic capacitor at C9
- ☐ Install 10 nF radial ceramic capacitors at C1, C16
- ☐ Install resistor packs at RP1, RP2
- ☐ Install DIP switches at SW2, SW3
- ☐ Install five 22 µF 16 V radial electrolytic capacitors at C25 - C29
- ☐ Install TO-92 DS1233 at U1
- ☐ Hairpin bend all 1 kΩ resistors and install at R21, R22
- ☐ Install three previously hairpinned 4.7 kΩ resistors at R3, R4, R20
- ☐ Install three LEDs at D1, D2, D3
- ☐ Break the 22-pin pin header strip into two 8-pin sections and two 3-pin sections
- ☐ Install two 3-pin header sections at J1, J2
- ☐ Install two 8-pin header sections next to one another at J5
- ☐ Install 4 MHz CPU clock crystal at Y1
- ☐ Install 2.4576 MHz serial clock crystal at Y2

3.3 Insert Socketed ICs

- ☐ Insert SRAM into sockets at U15, U16
- ☐ Insert 8085 CPU into socket at U9
- ☐ Insert 28C256 EEPROM into socket at U17
- ☐ Insert 8251A USART into socket at U19
- ☐ Insert MAX232 level shifter into socket at U21

3.4 Solder Console Cable

Glitch Works parts kits include a DB25F connector for the 8085 SBC rev 3 console cable, as well as a one-foot pigtail terminated in a 5-pin Molex KK-100 connector. This pigtail connects to J6, `RS-232 CONSOLE`. Use the following table to build a console cable appropriate to your intended terminal:

J6 Pin	DB25F DCE Pin	DB25F DTE Pin	Function
1	5	4	Request to Send
2	3	2	Transmit Data
3	2	3	Receive Data
4	4	5	Clear to Send
5	7	7	Signal Ground

J6 pin 4, `CTS` *must* be asserted for the console USART to transmit data. `RTS` may be left unconnected if hardware handshaking is not desired. Console pigtails provided with Glitch Works parts kits omit pin 1, `RTS`.

A serial light box will help debug potential serial wiring problems, we highly recommend the addition of a light box to your toolkit if you regularly interface RS-232 equipment. Our personal favorite is the IQ Technologies SmartCable SC821 Plus.

4 Initial Checkout and Testing

Once the 8085 SBC rev 3 is assembled, configure it as described in the "Configuration" section, starting on Page 2. Make sure that `RPA2 - RPA0` (SW2, positions 6-8) are all open.

Double-check all ICs for proper orientation, check all solder joints for cold joints or solder bridges. Connect the power pigtail provided to a suitable regulated 5 V power supply capable of providing at least 500 mA. Connect your serial terminal or computer to the console port. Apply power to your system and press `RESET`. The GWMON sign-on message should be printed to the console, and GWMON should respond to appropriate user input. `POWER ON` and `ROM ON` LEDs D1 and D2 should be lit.

4.1 Troubleshooting

If your 8085 SBC rev 3 fails to come up, recheck all solder joints for cold joints, bridges, or missed pins – this is by far the most common problem we've observed during assembly workshops. Recheck configuration options. Ensure your serial terminal or terminal emulator software is properly configured and that your cable is wired correctly (a RS-232 light box is very helpful here). The Intel 8251A *must* have `CTS` asserted or it will disable its transmitter and refuse to send characters.

Verify that `*BRESET` is properly strobing during power-up and when pressing the `RESET` button (SW1). If the `ROM ON` (D2) LED does not light after reset, either the power-on options for ROM (J1 and J2) are incorrect, or the flip-flop circuit is faulty.

4.2 Repair and Service

If you purchased an assembled 8085 SBC rev 3 from The Glitch Works, your board is warranted to work on arrival. If you have assembled a kit that fails to work, you may return it to The Glitch Works for evaluation, repair, and testing. For questions concerning returns or configuration, please visit `http://www.glitchwrks.com/` and click the "Contact" link.

Do note that while we will attempt to help those who have purchased used boards, there is no warranty extended.

5 Technical Notes

5.1 Board Control Register

The 8085 SBC rev 3 includes a board control register, which is a series of writable latches that affect how various parts of the built-in circuitry function. This register is addressed at `I/O BASE + 0x02`; in the default configuration, this places the board control register at `0x02`. Electrically, it is composed of three different latches: a 4-bit D-type latch at U2, and two elements of a dual D-type latch at U3. The bits of the board control register are mapped as follows:

Register Bit	Function	Notes
0	ROM Page Address, bit 0	Cleared on reset
1	ROM Page Address, bit 1	Cleared on reset
2	ROM Page Address, bit 2	Cleared on reset
3	ROM Boot flip-flop	Reset state determined by J1
4	ROM Enabled flip-flop	Reset state determined by J2
5	Unused	
6	Unused	
7	`USER` LED output	Cleared (LED off) on reset

Bits 0-2 control the selected 4K page of ROM available at `ROM BASE`. These bits are cleared on reset so that the first page of ROM is available for booting. Writing to these bits immediately changes the ROM page. The state of these bits is available through the Board Status Register.

Bit 3 controls the ROM Boot flip-flop. When set, ROM is addressed at all memory locations, repeating throughout memory. This allows the 8085 to read ROM code at `0x0000` on reset. Writing a 0 to this bit clears it and immediately switches off the ROM Boot functionality. Typically, ROM boot code should contain a jump to a startup routine in ROM, which should immediately clear the ROM Boot bit. The reset state of bit 3 is controlled by J1, see the "Configuration" section for more information. The state of these bits is available through the Board Status Register.

Bit 4 enables ROM when set, and disables ROM when cleared. This allows unmapping ROM for use of the full 64 KB of system memory. Writing a 0 to this bit clears it and immediately switches off ROM, writing a 1 to this bit switches ROM in. The selected ROM page is not affected. The reset state of bit 3 is controlled by J2, see the "Configuration" section for more information. The state of these bits is available through the Board Status Register.

Bits 5 and 6 are not implemented; that is, nothing responds to their state when writing to the Board Control Register.

Bit 7 is connected to the `USER` LED (D3). Writing a 1 to this bit lights the LED, writing a 0 turns the LED off. This bit is cleared on reset.

5.2 Board Status Register

The 8085 SBC rev 3 includes a board status register which provides the state of several bits of the Board Control Register, as well as `ROM OPT` (SW3) DIP switch settings. This register is addressed at `I/O BASE + 0x02`; in the default configuration, this places the board control register at `0x02`.

Electrically, it is composed of an octal tristate bus transceiver. The bits of the board status register are mapped as follows:

Register Bit	Function	Notes
0	RPA0 switch, SW3-8	Closed reads 1
1	RPA1 switch, SW3-7	Closed reads 1
2	RPA2 switch, SW3-6	Closed reads 1
3	ROM Boot status	Boot Enabled reads 1
4	ROM Enabled status	ROM Enabled reads 1
5	ROM Page Address latch, bit 0	
6	ROM Page Address latch, bit 1	
7	ROM Page Address latch, bit 2	

Bits 0-2 reflect the state of SW3 positions 8 through 6. These positions are labeled `RPA0 - RPA2` in the silkscreen. With the standard version of GWMON, these switches select the ROM-FS record to load into memory at reset. A 1 in a given bit position corresponds to a closed switch.

Bit 3 reflects the status of the ROM Boot flip-flop. ROM Boot is enabled when this bit reads 1.

Bit 4 reflects the status of the ROM Enabled flip-flop. ROM is enabled when this bit reads 1.

Bits 5-7 reflect the state of the ROM Page Address latch, which selects the currently addressed 4K page from ROM at U17.

5.3 Default Memory Map

Address Range	Contents
`0x0000 - 0x7FFF`	Static RAM, IC socket U15
`0x8000 - 0xEFFF`	Static RAM, IC socket U16
`0xF000 - 0xFFFF`	Static RAM, IC socket U16, when ROM is disabled
`0xF000 - 0xFFFF`	4K page of ROM, IC socket U19, when ROM is enabled

Onboard memory devices may be overlaid by external devices on the Glitchbus using the `*BMASK` signal.

5.4 Default I/O Map

I/O Address	R/W	Function
`0x00`	R/W	USART Data Register
`0x01`	R	USART Status Register
`0x01`	W	USART Control Register
`0x02`	R	Board Status Register
`0x02`	W	Board Control Register
`0x03`	R	Board Status Register
`0x03`	W	Board Control Register

Note that the Board Control Register and Board Status register appear at both `0x02` and `0x03`.

6 Errata and Clarifications

6.1 Resistor Pack Values

Kits provided at VCF East XIII (May 2018) included 18 kΩ resistor packs for both RP1 and RP2. 18 kΩ was discovered to be insufficient for 74LS85 address comparators, resulting in SW3 1-4 being ignored (`ROM BASE` always at `0xF000`). All later parts kits include 10 kΩ or smaller resistor packs for both positions. Thanks to Josh Bensadon for reporting this error!

6.2 ROM Compatibility

The ROM socket at U17 is compatible with JEDEC standard 32K x 8 static RAM, Ferroelectric RAM (FeRAM), and 28C256 EEPROMs. It may not be compatible with some manufacturers' UV EPROMs, such as the common 27256 EPROM.

7 Parts List

The following substitutions may be made if you have purchased a bare board and are supplying your own parts, or in a full Glitch Works parts kit:

- Any compatible 7400 series family logic ICs may be used (for example, a 74LS04 in the parts list may be shipped as a 7404, 74S04, 74F04, 74LS04, 74ALS04, or 74HCT04)
- All 4.7 kΩ resistors and resistor packs on the GW-OSI-RAM1 are pull-up or pull-down resistors, and may be any value from 2.2 kΩ to 10 kΩ, even though they are indicated as 4.7 kΩ on the assembly drawing
- Resistors may be of varying precision and body type

If you purchased a full Glitch Works parts kit, be sure it includes the following:

☐ 1x 20 pF radial ceramic capacitor

☐ 19x 0.01 µF axial ceramic capacitor (yellow bead)

☐ 2x 10 nF 16 V radial ceramic capacitor

☐ 2x 22 µF 10 V axial tantalum capacitor

☐ 5x 22 µF 16 V radial electrolytic capacitor

☐ 3x 330 Ω 1/4 W resistor

☐ 2x 1 kΩ 1/4 W resistor

☐ 17x 4.7 kΩ 1/4 W resistor (see above note)

☐ 2x 10 kΩ x 9 SIP resistor packs (see note above)

☐ 1x 4 MHz crystal

☐ 1x 2.4576 MHz crystal

☐ 1x 8085 CPU

☐ 1x 8251A USART

☐ 1x 28C256 EEPROM, preloaded with GWMON

☐ 2x JEDEC 62256-type 32K x 8 static RAM

☐ 1x 74LS00 quad 2-input NAND gate

☐ 1x 74LS04 hex inverter

☐ 1x 74LS20 dual 4-input NAND gate

☐ 1x 74LS32 quad OR gate

☐ 1x 74LS74 dual D-type flip flop

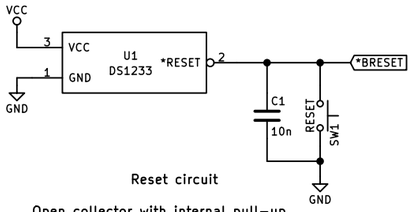
☐ 1x 74LS85 4-bit comparator

☐ 1x 74LS138 1-of-8 decoder

☐ 1x 74LS175 quad D-type latch

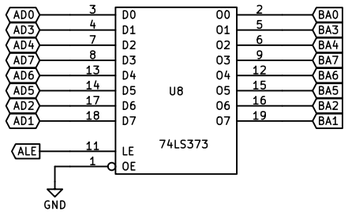
- ☐ 3x 74LS245 tranceiver
- ☐ 1x 74LS373 octal D-type latch
- ☐ 1x 74LS688 magnitude comparator
- ☐ 1x 74HCT4040 12-stage binary counter
- ☐ 1x MAX232 RS-232 level shifter
- ☐ 1x DS1233 EconoReset
- ☐ 2x 8-position DIP switch
- ☐ 3x red T-5 LED
- ☐ 1x mini tact pushbutton switch
- ☐ 1x 22-pin breakaway header strip
- ☐ 2x jumper shunt
- ☐ 1x 2-position Molex KK-100 header
- ☐ 1x 5-position Molex KK-100 header
- ☐ 4x 28-pin IC socket
- ☐ 1x 16-pin IC socket
- ☐ 1x Power pigtail
- ☐ 1x RS-232 console pigtail
- ☐ 1x DB25F connector

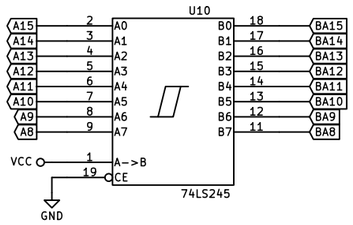
J1: 1-2 ROM BOOT DISABLED
2-3 ROM BOOT ENABLED
J2: 1-2 ROM DISABLED AT RESET
2-3 ROM ENABLED AT RESET
8085 SBC rev 3 (c) 2018 The Glitch Works
http://www.glitchwrks.com/8085projects
C25-C29: 1 TO 22 uF
8085 CPU
74LS373
74LS688
74LS245
74LS175
74LS74
74LS00
74LS32
74LS20
74LS138
74LS85
74LS04
74LS4040
8251A USART
74LS245
32K ROM OR EEPROM
62256 SRAM
62256 SRAM
74LS245
MAX232
ROM OPTION SWITCHES
I/O BASE ADDRESS SWITCHES
GLITCHBUS EXPANSION
RS-232 CONSOLE
GND CTS RX TX RTS
POWER
GND +5V
UART SPEED
38400 19200 9600 4800 2400 1200 600 300
4 MHz
2.4576 MHz
22 uF
22 uF
10n
DS1233
RESET SW1
POWER ON
ROM ON
USER
INTERRUPT
A15 A14 A13 A12 WR RPA2 RPA1 RPA0
A7 A6 A5 A4 A3 A2



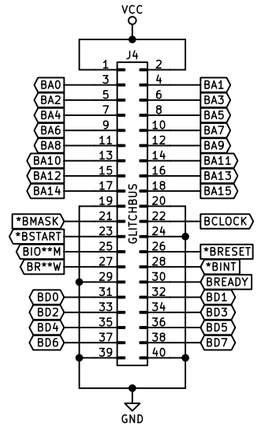
Reset circuit

Open collector with internal pull-up
Can connect an external switch from Glitchbus

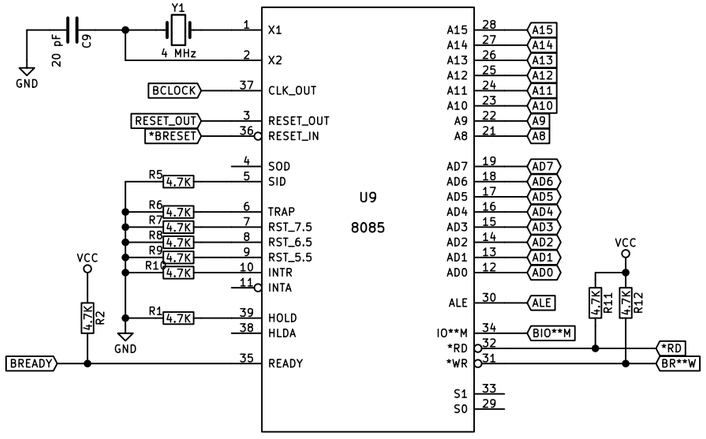




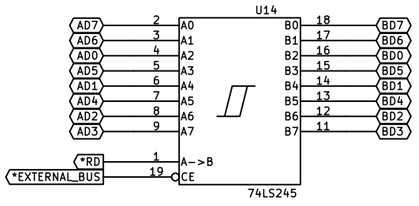
Address Latch and Buffering



Glitchbus Expansion Connector

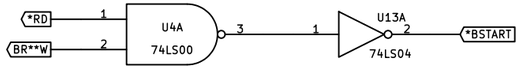


Processor, Oscillator, and Pull-Ups/Pull-Downs

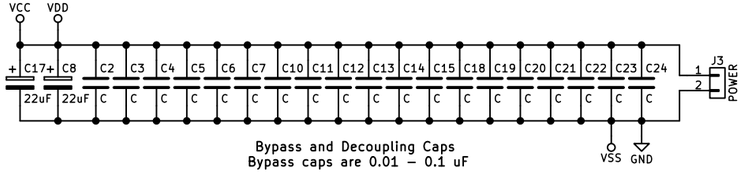


Data Bus Buffer and Control Logic

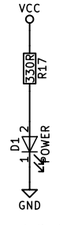
External data bus is only active when no onboard device is selected



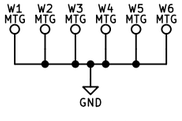
*BSTART Signal Generator -- Signals Start of Bus Transaction



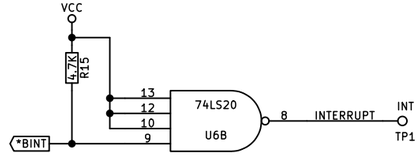
Bypass and Decoupling Caps
Bypass caps are 0.01 - 0.1 uF



Power Indicator



Mounting Holes



Interrupt Inverter

If desired, jumper output to one of the 8085 interrupt inputs
Recommended to use a half-interrupt, not INTR

UART and I/O

uart_io.sch

Memory Devices

memory.sch

J. Chapman
The Glitch Works
Sheet: /
File: 8085_sbc_rev3.sch

Title: 8085 SBC rev 3

Size: USLedger	Date: 2018-07-01	**Rev: 1**
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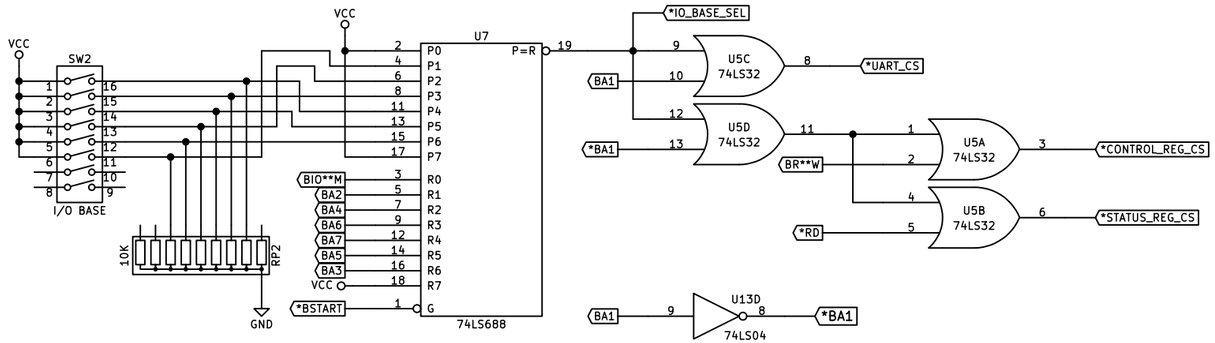
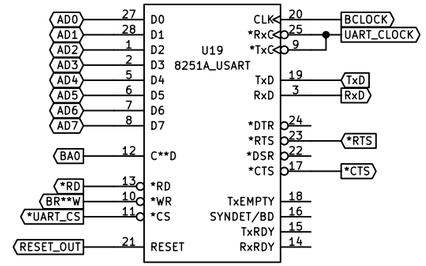
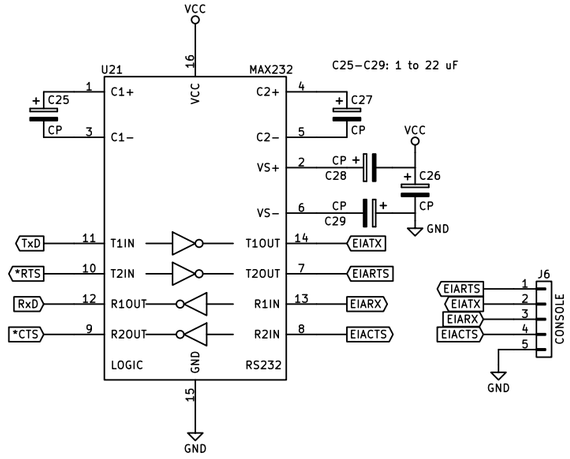


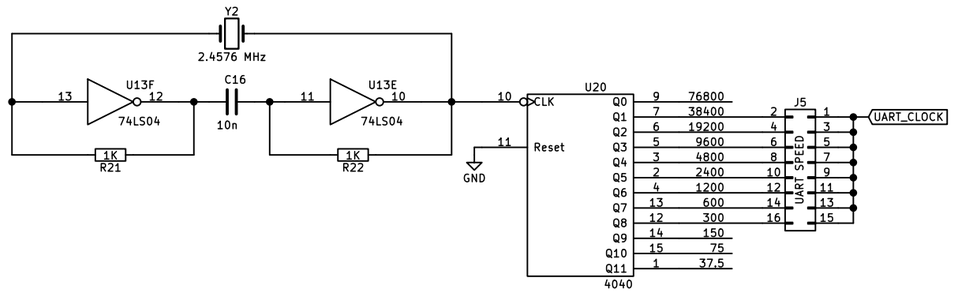
I/O Base Address and Device Select Decode Logic



8251A USART



RS–232 Level Shifter



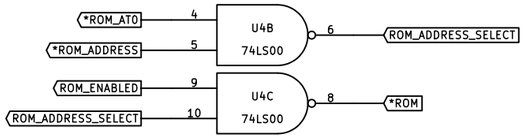
UART Clock Generator

J. Chapman
The Glitch Works

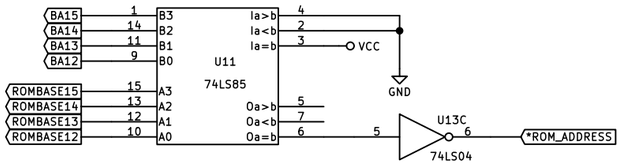
Sheet: /UART and I/O/
File: uart_io.sch

Title: 8085 SBC rev 3

Size: USLedger	Date: 2018–07–01	**Rev: 1**
KiCad E.D.A. kicad 4.0.4–stable		Id: 2/3

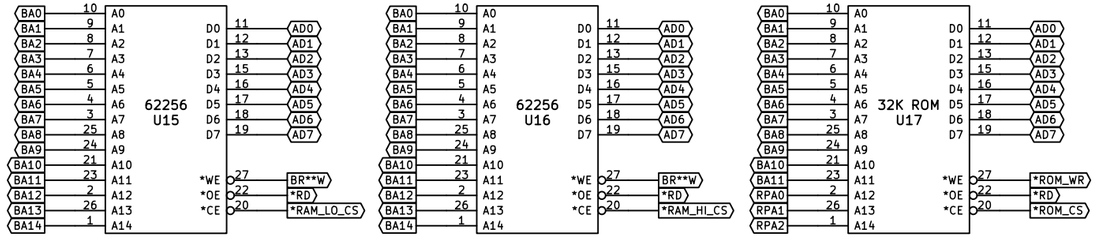


ROM Address Select Logic

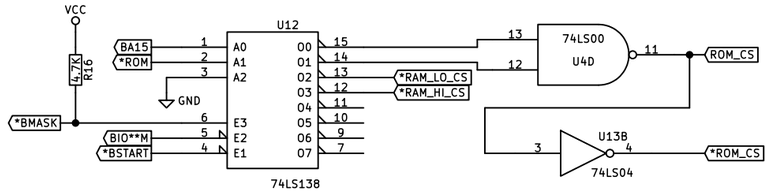


ROM Base Address Decoder

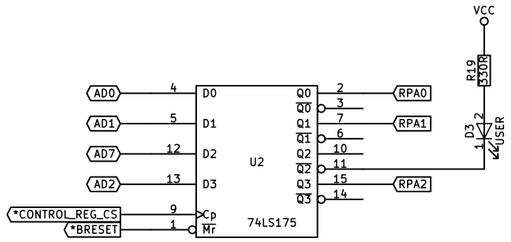
Determines the address of the 4K segment that ROM normally occupies when enabled and boot flip-flop is CLEAR



Memory Devices

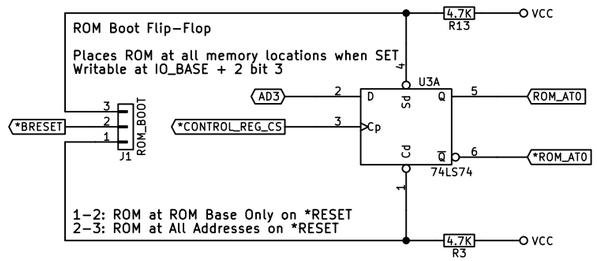


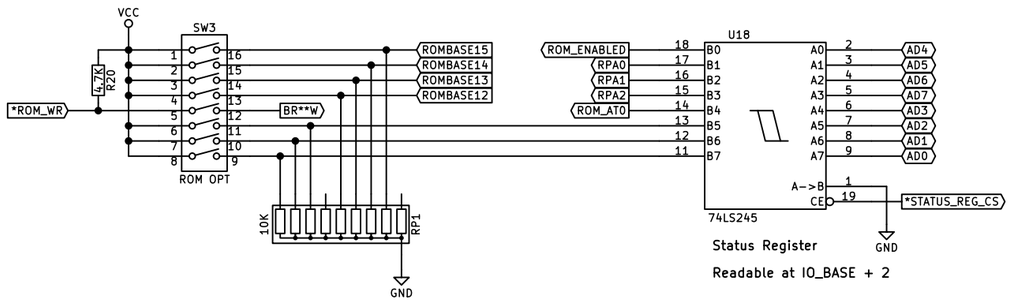
Memory Device Select Logic



ROM Page Register

This register controls which 4K page of ROM is addressed.
Cleared to 0 on *RESET, writable at IO_BASE + 2
Bits 0 – 2 set ROM page, bit 7 is user-defined





J. Chapman
The Glitch Works

Sheet: /Memory Devices/
File: memory.sch

Title: 8085 SBC rev 3

Size: USLedger	Date: 2018-07-01	**Rev: 1**
KiCad E.D.A. kicad 4.0.4-stable		Id: 3/3