Glitch Works GW-OSI-RAM1

User's Manual and Assembly Guide

Revision 1, 2017-09-04

http://www.glitchwrks.com/

Contents

1 Introduction

The Glitch Works GW-OSI-RAM1 is a universal RAM/ROM board for the Ohio Scientific bus. It includes the following features:

- Fully static operation
- No expensive or hard-to-get components (8T26 buffers, etc.)
- 8- and 12-bit support
- Support for inverted and non-inverted data bus
- Optional bank switching
- ROM support/overlay
- Mappable around existing RAM, ROM, and I/O in 4K segments
- Header for lamp register
- General purpose prototype area

The GW-OSI-RAM1 uses JEDEC pinout 32K x 8 memory devices, such as the 62256 SRAM, 27256 EPROM, or 28256 EEPROM. Memory can be enabled in 4K segments to map around existing RAM, ROM, and I/O. The board can be configured to mix RAM and ROM in two separate banks. It can be used with any system that uses the Ohio Scientific bus, including the SYS bus of the Ohio Scientific 560Z Processor Lab. Full 12-bit operation allows it to be used with the OSI 560Z in PDP-8 compatible mode.

2 Configuration

Due to its flexibility, the GW-OSI-RAM1 contains a large number of DIP switches and several jumpers. Memory management requires jumper wires to be inserted. The following table explains switch and jumper function. Please refer to the assembly drawing for the locations of switches and jumpers.

Name	Function
SW1	First bank 0-32K, each position enables a 4K segment when ON
SW2	First bank 32-64K, each position enables a 4K segment when ON
SW3	Second bank 0-32K, each position enables a 4K segment when ON
SW4	Low byte of I/O address, ON = 1
SW5	High byte of I/O address, ON = 1
SW6	Second bank 32-64K, each position enables a 4K segment when ON
J1	I/O address size selection, 1-2 for 1 byte, 2-3 for 2 bytes
J2	I/O address decode enable, closed enables I/O decode

For instance, if you wished to enable 12K of RAM starting at `0x0000` in the first bank, close positions 1, 2, and 3 of SW1.

Any memory segment that contains RAM, ROM, or I/O on another board should have its segment disabled on the GW-OSI-RAM1. Consult your system's documentation to determine which segments are in use for the system and board set you have. Generally, the 4K segment at `0xF000` will be required for I/O devices and boot ROMs, and should be disabled on the GW-OSI-RAM1. Video systems should disable the two 4K segments at `0xD000` and `0xE000`. Systems with ROM BASIC should disable the two 4K segments at `0xA000` and `0xB000`.

For systems that include RAM on the CPU board, you must either disable the RAM on the CPU board and use only the RAM on the GW-OSI-RAM1, or disable the segments occupied by CPU board RAM. The procedure for disabling CPU board RAM will depend on the particular CPU board in use. It is usually easier to disable those segments on the GW-OSI-RAM1, unless there are suspected reliability problems with the CPU board's onboard RAM.

2.1 Configuring I/O

SW4, SW5, J1, and J2 control I/O configuration. If no I/O is desired, remove the shunt from J2 – all other I/O settings will be ignored if J2 is open.

If J2 is closed, SW4 specifies the low byte of the I/O address, while SW5 specifies the upper byte. If the I/O device is write-only (for example, a GW-OSI-HLR1 Hex Lamp Register), it can be addressed over existing RAM on the GW-OSI-RAM1 *but not on another RAM board*. If the I/O device is read-only or read/write, it must not overlap RAM. The GW-OSI-RAM1 provides memory management inputs in the memory address decoding sections to allow a read-only or read-write I/O device to be inserted into RAM on the GW-OSI-RAM1. These memory management inputs will not work for RAM on other boards.

J1 selects the I/O size. Placing a shunt between pins 1 and 2 set it to one byte, a shunt between pins 2 and 3 set it two two bytes. Determine this setting from the module you plan to install in J3, or your own needs if using the prototype area.

2.2 Memory Management

The GW-OSI-RAM1 supports Ohio Scientific 1 MB memory management, which is implemented on some OSI CPU boards, such as the OSI 510. Most smaller systems will not use memory management and will be limited to 64K of RAM, ROM, and I/O devices.

If OSI 1 MB memory management is not being used, the second bank on the GW-OSI-RAM1 can be used for ROM overlays. This allows mixing RAM and ROM on the same board, in 4K segments. Resistors R2 - R7 control which banks are active by default, and must be configured for ROM overlays, if desired. The following table describes possible configurations of R2 - R7:

Resistors Installed	Function
R2, R3	Default configuration, first bank enabled at `0x0000` - `0xFFFF`
R4	Second bank 0-32K enabled, used for ROM overlay
R6	Second bank 32-64K enabled, used for ROM overlay
R5	Second bank 0-32K to be controlled by custom memory management
R7	Second bank 32-64K to be controlled by custom memory management

For a 64K system with no memory management, R2, R3, R4 and R6 are installed, allowing 0-64K of RAM with 0-64K of ROM overlays. For a system with memory management, R2, R3, R5, and R7 are installed, and jumper connections are made from U3 and/or U6. Consult the schematics for 1 MB memory management jumpering.

2.3 Prototyping Area

A prototyping area is provided on the GW-OSI-RAM1, and can be used whether or not a mezzanine expansion module is to be installed, provided devices under the mezzanine module are short enough. The prototyping area consists of a section of plated-through holes, sized to fit the leads of a 2 W resistor without drilling. This allows multiple wires to be inserted in a single hole, making point-to-point prototyping very easy.

Header J3 provides buffered data lines, address lines `A0` and `A1`, and read/write signals for both the mezzanine modules and prototyping space. The `*IOSEL` signal is used by mezzanine modules, but may be used by the prototype area if no mezzanine module is installed, or if the circuitry in the prototype area is designed to co-exist with the mezzanine module in use.

Consult the schematics for J3 pinout and signal functions.

2.4 12-Bit Operation

The GW-OSI-RAM1 was designed with 12-bit operation in mind, for use on the SYS bus of the OSI 560Z Processor Lab. Addressing and configuration is the same as 8-bit mode, but the data buffer at U24 must be installed, and RAM or ROM must be installed in U14 - U17 to provide the additional upper 4 data bits. Refer to the assembly drawing for addresses covered by U14 - U17.

While extended memory management is techincally possible in 12-bit mode, no current boards implement it.

Expansion connector J3 supports 12-bit data operation, and modules such as the GW-OSI-HLR1 Hex Lamp Register will display 12-bit data if the system controlling the GW-OSI-RAM1 supports it. Leaving 12-bit operation enabled when using the GW-OSI-RAM1 in an 8-bit system is acceptable, as long as the four additional data lines used in 12-bit operation are not used for other purposes. Consult your system documentation and/or schematics to determine this. If in doubt, remove the data buffer at U24 to disable 12-bit operation.

2.5 Inverted and Non-Inverted Data Busses

The GW-OSI-RAM1 can be used with either inverted or non-inverted data busses. Inverted busses are typically found on larger or later OSI systems, which non-inverted data busses are found on some of the smaller and earlier OSI systems. Most OSI boards can be configured for either operation.

Data bus polarity does not matter if the GW-OSI-RAM1 will only be used for RAM; however, it should match the system's data bus polarity if using ROM, mezzanine modules, or the prototyping area. The following table describes which buffers should be used in U24, U27, and U28:

Bus Polarity	Buffers on CPU Board	Buffers in U24, U27 and U28
Inverted	8T26 or MC6880	74LS240
Non-Inverted	8T28 or MC6889	74LS244

3 Assembly

The GW-OSI-RAM1 is designed to be easy to assemble for anyone with moderate soldering ability. The following tools will be required:

- Soldering iron, 20-40 W recommended, grounded tip
- Solder, 63/37 leaded solder recommended, Kester "44 Core" or similar
- Diagonal cutters or flush cutters
- Solder braid, solder sucker, or desoldering station, in the event errors are made
- Needle-nose pilers for bending component leads
- 1/4 and 1/8 W resistor lead forms (optional)

This manual does not cover basic soldering technique. If you are new to soldering, we recommend the Adafruit soldering guide and plenty of practice on a piece of protoboard, before beginning assembly of the GW-OSI-RAM1. The Adafruit guide can be found at:

`https://learn.adafruit.com/adafruit-guide-excellent-soldering`

3.1 Assembling the GW-OSI-RAM1

If you purchased a full Glitch Works parts kit, we recommend completing all assembly sections, since extra features can be disabled as needed. If supplying your own parts, you may choose which sections to complete based on the functionality required.

Note that pin 1 is designated with a square pad for all ICs, diodes, resistor packs, switches, and connectors. Pin 1 faces away from the OSI bus connector for all ICs, diodes, resistor packs, and switches. The component (top) side of the board is the side which contains the Open Source Hardware gear logo. The following steps should always be completed:

☐ Verify parts list against kit contents or builder-provided parts

☐ Consult the assembly drawing for component locations and values

☐ Bend all 0.01 µF bypass capacitors (yellow axial bead) – position 2 on a 1/8 W lead form

☐ Install all 0.01 µF capacitors in positions marked C in assembly diagram

☐ Bend and install 1N4148 diode at D1 – position 4 on a 1/8 W lead form

☐ Install 74LS245 address buffers at U22, U23

☐ Install 74LS30 at U25

☐ Install 74LS00 at U26

☐ Install 74LS04 at U9

☐ Install resistor pack at RN7

☐ Install 20-pin IC sockets at U27, U28

☐ Install 22 µF 10V capacitor at C25, bend leads with needle-node pliers

☐ Install four 12-pin Molex connectors at the board edge connector

3.2 0-64K Memory, no Memory Management or ROM Overlay

The following components should be installed for a 0-64K system without memory management or ROM overlay:

- ☐ Install 74LS138 decoders at U1, U4
- ☐ Install 74LS30 ICs at U2, U5
- ☐ Install DIP switches at SW1, SW2
- ☐ Install resistor packs at RN1, RN2
- ☐ Bend two 10K resistors – position 1 on a 1/4 W lead form
- ☐ Install 10K resistors at R2, R3
- ☐ Install two 28-pin sockets at U20, U21

Complete the following steps *only if no memory management or ROM overlay will be used*:

- ☐ Cut and bend two wire jumpers to link IC pads 7 and 8 on a 14-pin DIP IC – clipped capacitor leads work well
- ☐ Install wire jumpers on U8, U11, across pads 7 and 8

3.3 Memory Management or ROM Overlay Support

Complete the above sections, being sure not to install wire jumpers across U8 and U11, then install the following:

- ☐ Install 74LS138 decoders at U7, U10
- ☐ Install 74LS30 ICs at U8, U11
- ☐ Install DIP switches at SW3, SW6
- ☐ Install resistor packs at RN1, RN2
- ☐ Install two 28-pin sockets at U18, U19
- ☐ Bend two 10K resistors – position 1 on a 1/4 W lead form
- ☐ Consult the table on Page 3 of this manual and install 10K resistors at the positions required for your needs

If OSI 1 MB memory management is required, complete the following steps:

- ☐ Install 74LS138 decoders at U3, U6
- ☐ Jumper outputs from U3 and/or U6 to memory management inputs on U7 and/or U10 – consult schematic

3.4 I/O Support

To enable support for an I/O mezzanine module or for use with the prototype area, complete the following steps. Note that I/O can be disabled by jumper shunt if this section is populated:

- ☐ Install 74LS688 comparators at U12, U13
- ☐ Bend one 10K resistor – position 1 on a 1/4 W lead form
- ☐ Install 10K resistor at R8
- ☐ Install DIP switches at SW4, SW5
- ☐ Install resistor packs at RN4, RN5
- ☐ Install a three-pin jumper header at J1
- ☐ Install a two-pin jumper header at J2
- ☐ Install 20-pin header socket at J3, if mezzanine modules will be used

Complete the following steps *only if the board will be used for I/O only (no memory at all)*:

- ☐ Cut and bend four wire jumpers to link IC pads 7 and 8 on a 14-pin DIP IC – clipped capacitor leads work well
- ☐ Install wire jumpers on U2, U5, U8, U11, across pads 7 and 8

3.5 12-Bit Support

If 12-bit operation is required for either memory or I/O, complete the following steps:

- ☐ Bend four 10K resistors – position 1 on a 1/4 W lead form
- ☐ Install 10K resistors at R9 - R12
- ☐ Install 20-pin IC socket at U24
- ☐ Install 28-pin IC sockets at U16, U17 for 64K memory support with no memory management or ROM overlay
- ☐ Install 28-pin IC sockets at U14, U15 for memory management or ROM overlay

3.6 Insert Socketed ICs

- ☐ Insert SRAM or ROM devices into appropriate sockets – consult assembly drawing
- ☐ Insert 74LS240 or 74LS244 bus drivers into U24, U27, U28 – choose ICs based on the table on Page 4

4 Initial Checkout and Testing

Once the GW-OSI-RAM1 is assembled, configure it as described in the "Configuration" section, starting on Page 2. It is recommended that initial testing be done with a minimum board set, and boards reinstalled after operation is confirmed.

Double-check all ICs for proper orientation, check all solder joints for cold joints or solder bridges. Insert the GW-OSI-RAM1 into your system's backplane – this will require significant force, especially the first time that the board is installed. If using a system with a horizontal card cage, support the GW-OSI-RAM1 with a spacer in the corner hole near the "OSI Universal 128KW RAM Board" text. Apply power to your system and press `RESET`. Using the ROM monitor, BASIC's auto-size function, or a dedicated RAM test program, verify that the RAM configured on the GW-OSI-RAM1 is detected and functioning.

4.1 Troubleshooting

If your system fails to come up with the GW-OSI-RAM1 installed, start by disabling all memory segments – set SW1 - SW3 and SW6 to all off. Remove the jumper shunt on J2, if installed. If this allows the system to come up, start enabling RAM segments one at a time, to determine where a conflict may exist.

If setting all segment switches to off and opening J2 does not allow the system to come up, it is likely that the bus tranceivers are being turned on when they should be off. This can occur if any of U2, U5, U8, or U11 are not installed and no jumper has been placed across pins 7 and 8. It can also occur if RN7 is not installed properly or if diode D1 is installed backwards. Recheck assembly and try again.

4.2 Repair and Service

If you purchased an assembled GW-OSI-RAM1 from The Glitch Works, your board is warranted to work in a system that is otherwise fully operational. If you have assembled a kit that fails to work, you may return it to The Glitch Works for evaluation, repair, and testing. For questions concerning returns or configuration, please visit `http://www.glitchwrks.com/` and click the "Contact" link.

Do note that while we will attempt to help those who have purchased used boards, there is no warranty extended.

5 Parts List

The following substitutions may be made if you have purchased a bare board and are supplying your own parts, or in a full Glitch Works parts kit:

- Any compatible 7400 series family logic ICs may be used (for example, a 74LS04 in the parts list may be shipped as a 7404, 74S04, 74F04, 74LS04, 74ALS04, or 74HCT04)
- All resistors and resistor packs on the GW-OSI-RAM1 are pull-up or pull-down resistors, and may be any value from 4.7K to 47K, even though they are indicated as 10K on the assembly drawing
- Resistors may be of varying precision and body type – they are all the same on the GW-OSI-RAM1 and can be used in any position

If you purchased a full Glitch Works parts kit, be sure it includes the following:

☐ 28x 0.01 µF axial ceramic capacitor (yellow bead)

☐ 9x 10K 1/4 W resistor (see above note)

☐ 1x 1N4148 diode

☐ 1x 22 µF 10V axial tantalum capacitor

☐ 7x 10K x 9 SIP resistor packs (see note above)

☐ 2x 74LS245 tranceiver

☐ 3x 74LS240 inverting bus tranceiver

☐ 1x 74LS00 quad 2-input NAND gate

☐ 1x 74LS04 hex inverter

☐ 5x 74LS30 8-input NAND gate

☐ 6x 74LS138 1-of-8 decoder

☐ 2x 74LS688 magnitude comparator

☐ 2x JEDEC 62256-type 32K x 8 static RAM

☐ 6x 8-position DIP switch

☐ 1x 2-pin jumper header

☐ 1x 3-pin jumper header

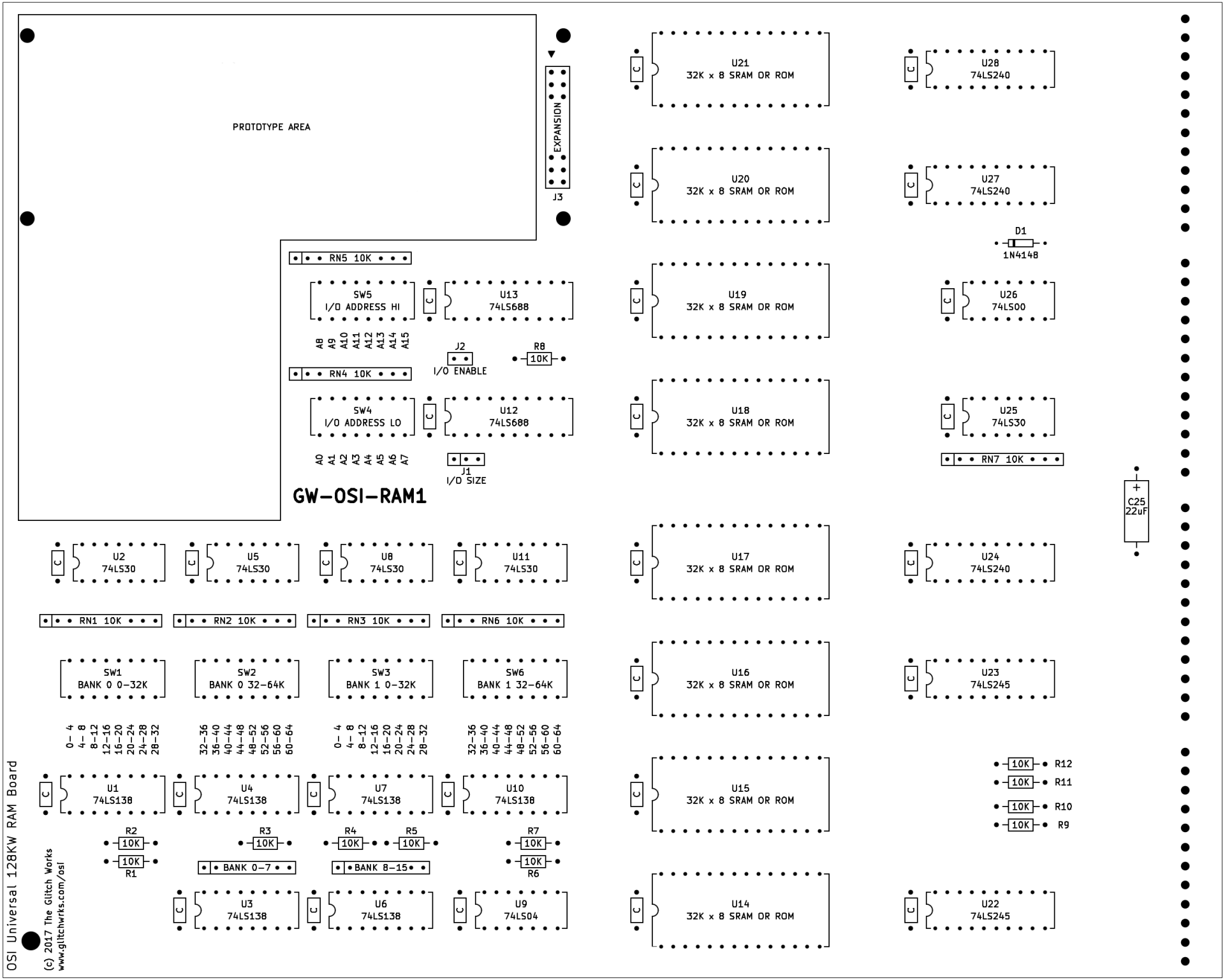
☐ 2x jumper shunt

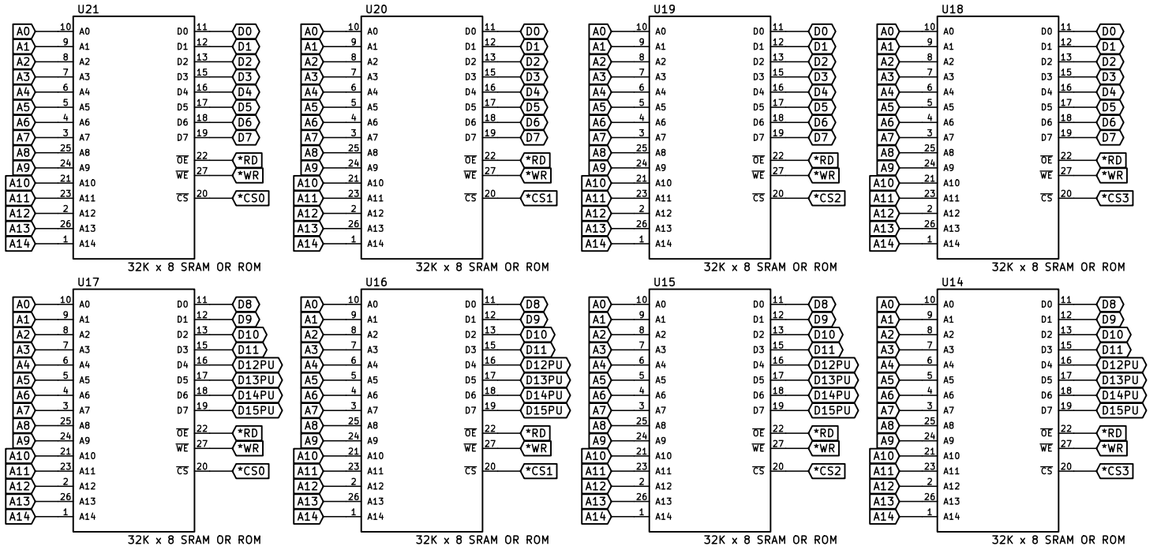
☐ 8x 28-pin IC socket

☐ 3x 20-pin IC socket

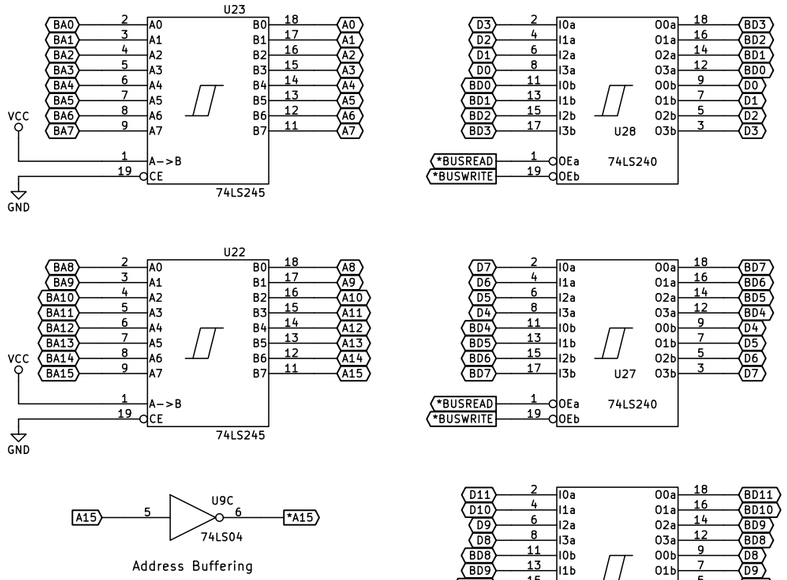
☐ 4x Molex KK-156 12-pin right angle connector

☐ 1x 20-pin header socket


PROTOTYPE AREA
EXPANSION
J3
RN5 10K
SW5
I/O ADDRESS HI
U13
74LS688
A8 A9 A10 A11 A12 A13 A14 A15
J2
I/O ENABLE
R8
10K
RN4 10K
SW4
I/O ADDRESS LO
U12
74LS688
A0 A1 A2 A3 A4 A5 A6 A7
J1
I/O SIZE
GW-OSI-RAM1
U2
74LS30
U5
74LS30
U8
74LS30
U11
74LS30
RN1 10K
RN2 10K
RN3 10K
RN6 10K
SW1
BANK 0 0-32K
SW2
BANK 0 32-64K
SW3
BANK 1 0-32K
SW6
BANK 1 32-64K
0- 4
4- 8
8-12
12-16
16-20
20-24
24-28
28-32
32-36
36-40
40-44
44-48
48-52
52-56
56-60
60-64
U1
74LS138
U4
74LS138
U7
74LS138
U10
74LS138
R2
10K
10K
R1
R3
10K
BANK 0-7
R4
10K
R5
10K
BANK 8-15
R7
10K
10K
R6
U3
74LS138
U6
74LS138
U9
74LS04
U21
32K x 8 SRAM OR ROM
U20
32K x 8 SRAM OR ROM
U19
32K x 8 SRAM OR ROM
U18
32K x 8 SRAM OR ROM
U17
32K x 8 SRAM OR ROM
U16
32K x 8 SRAM OR ROM
U15
32K x 8 SRAM OR ROM
U14
32K x 8 SRAM OR ROM
U28
74LS240
U27
74LS240
D1
1N4148
U26
74LS00
U25
74LS30
RN7 10K
C25
22uF
U24
74LS240
U23
74LS245
R12
10K
R11
10K
R10
10K
R9
10K
U22
74LS245
OSI Universal 128KW RAM Board
(c) 2017 The Glitch Works
www.glitchwrks.com/osi



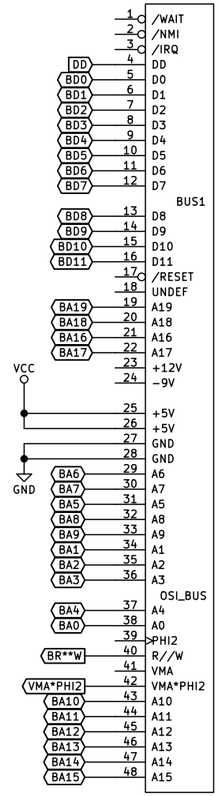
Memory Banks



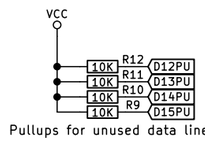
Address Buffering

Data Bus Tranceivers

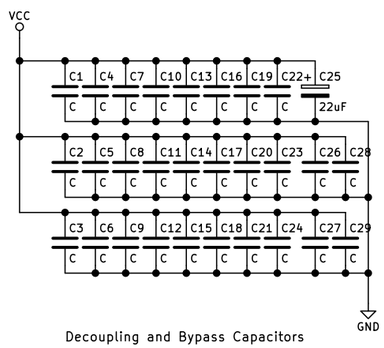
Pin 1 LOW = Internal Bus to MOS Bus
Pin 19 LOW = MOS Bus to Internal Bus



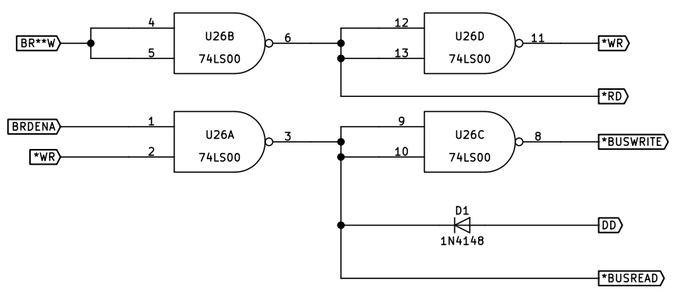
OSI Bus



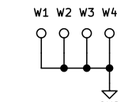
Pullups for unused data lines



Decoupling and Bypass Capacitors



*RD *WR Generation and Bus Buffer Control



Mezzanine Mounting Holes

I/O Circuits

io.sch

Decode Logic

decode.sch

http://www.glitchwrks.com/osi
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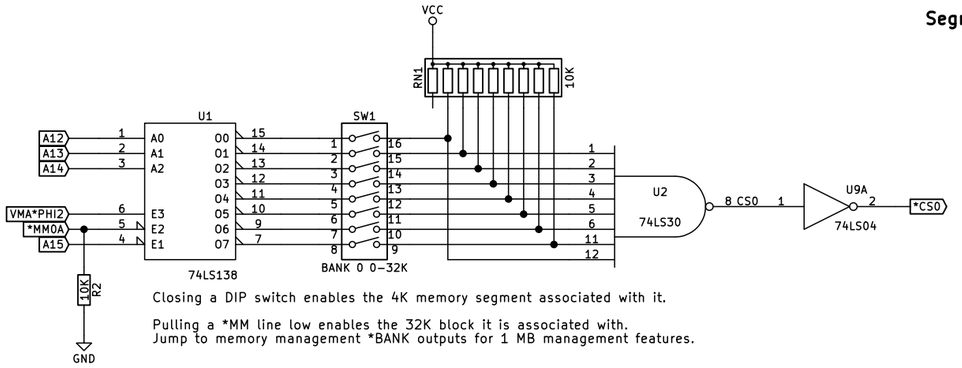
Sheet: /
File: osi_12bit.sch

Title: Ohio Scientific Universal RAM Board

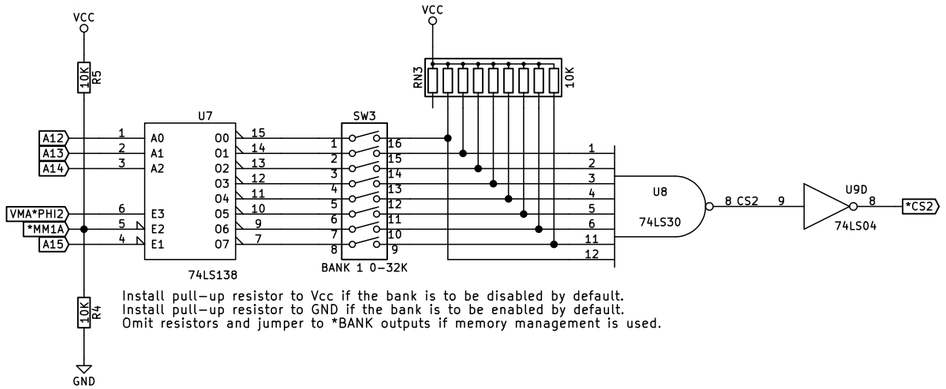
Size: USLedger	Date: 2017-09-04	**Rev: 1**
KiCad E.D.A. kicad 4.0.4-stable		Id: 1/3

Segment Select Logic

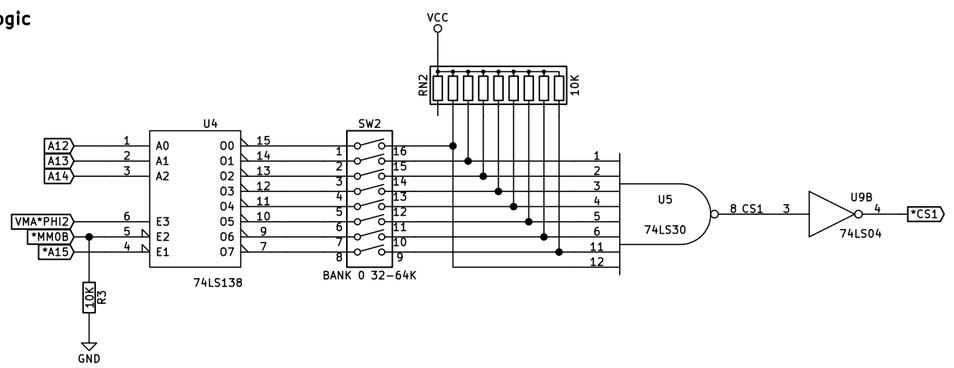


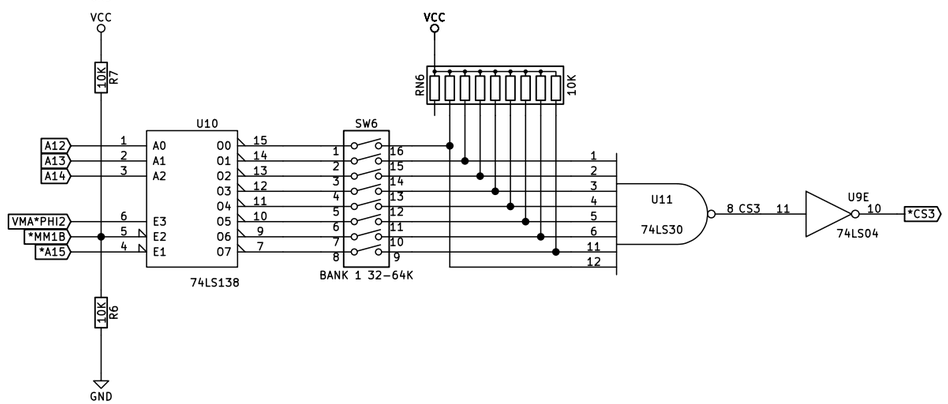
Closing a DIP switch enables the 4K memory segment associated with it.

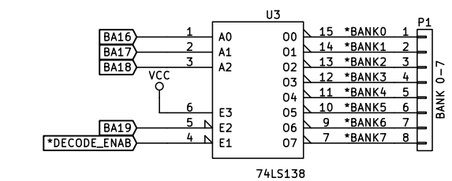
Pulling a *MM line low enables the 32K block it is associated with.
Jump to memory management *BANK outputs for 1 MB management features.

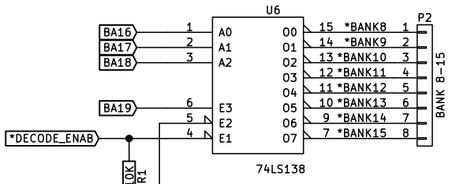


Install pull-up resistor to Vcc if the bank is to be disabled by default.
Install pull-up resistor to GND if the bank is to be enabled by default.
Omit resistors and jumper to *BANK outputs if memory management is used.





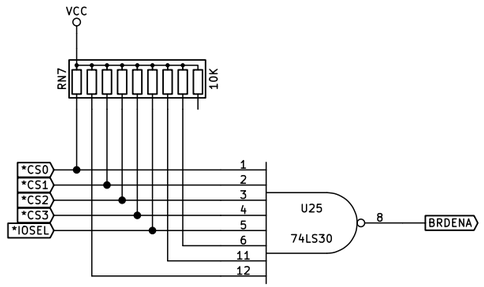




Extended Memory Management

Jump outputs to *MM input to enable
memory management up to 1 MB.

*DECODE_ENAB can be pulled low to disable
memory for memory-mapped I/O devices.



Board Enable Control

Bus buffers are active when any input goes low

http://www.glitchwrks.com/osi
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Sheet: /Decode Logic/
File: decode.sch

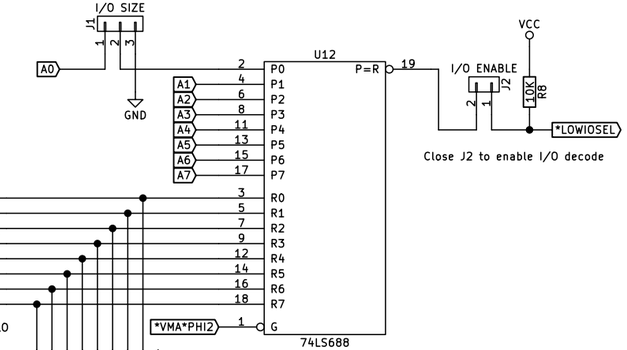
Title: Ohio Scientific Universal RAM Board

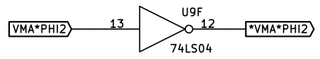
Size: USLedger	Date: 2017-09-04	**Rev: 1**
KiCad E.D.A. kicad 4.0.4-stable		Id: 2/3

NOTE: A write-only port (e.g. lamp register) may be overlaid with RAM which will provide a readback register. If using a readable port, *IOSEL must be jumpered to memory management inputs to disable the RAM address overlaid by the port.

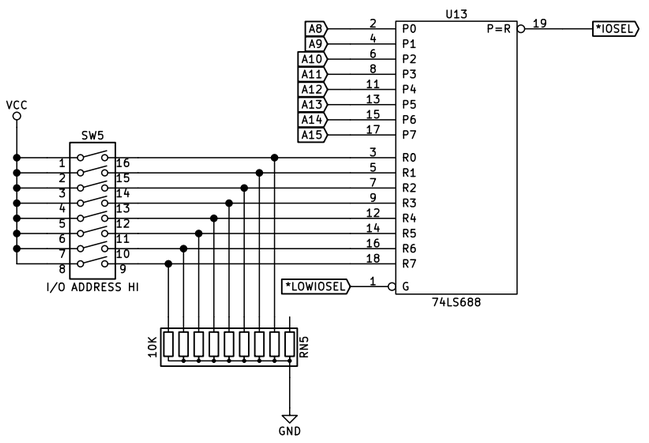
If using the I/O port in a segment with no RAM, jumper to a board enable pin on U25.

Jumper 1-2 for single I/O address, 2-3 for two I/O addresses.



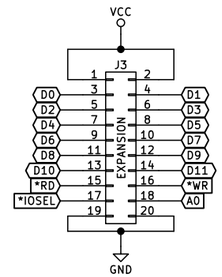


Low Address Select



High Address Select

Provides VMA*PHI2 conditioned address select.



Expansion Header

http://www.glitchwrks.com/osi
J. Chapman
The Glitch Works

Sheet: /I/O Circuits/
File: io.sch

Title: Ohio Scientific Universal RAM Board

Size: USLedger	Date: 2017-09-04	**Rev: 1**
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