Glitch Works R6501Q/R6511Q SBC
GW-R65X1QSBC-1

User's Manual and Assembly Guide

Revision 2, 2020-10-03

http://www.glitchwrks.com/

Contents

1 Introduction

The Glitch Works R6501Q/R6511Q (GW-R65X1QSBC-1) is a single-board computer (SBC) compatible with Rockwell's R6501Q and R6511Q one-chip microprocessors (referred to as the R65X1Q) in plastic QUIP (Quad Inline Package). The SBC is also compatible with the high speed A suffix Rockwell parts. It includes the following features:

- Rockwell R6501Q, R6511Q, R6501AQ, or R6511AQ
- 32 KB static RAM, FeRAM compatible
- 32 KB ROM, EEPROM, or FeRAM in 4K pages, in-board programmable
- Serial console via onboard UART
- ROM paging and switch-out
- Debounced reset and power supply supervisory circuit
- Glitchbus expansion header
- Glitchbus I/O mapped as a 256 byte memory page at `0xEF00`

The R65X1Q SBC includes a modified version of the eWoz monitor with customization for the R65X1Q onboard UART and memory layout. With the addition of a serial terminal (or terminal emulation software on a PC), the SBC provides a basic self-contained R65X1Q system. The SBC's ROM implementation is compatible with Glitch Works ROMFS, which allows for the storage of file records in ROM. These records can be loaded from the monitor, or automatically selected by option switches on reset/power-up. This also allows for in-board updates without overwriting the current, known-good copy of a program.

Two of the onboard R65X1Q parallel I/O ports are brought out to 5x2 pin headers on 0.1" centers. These ports are unused by the standard ROM software load and are available for user applications. See the R6500 applications manual specific to the processor used for more information.

2 Configuration

The R65X1Q SBC includes a switch pack and several optional resistors for configuring system options:

Name	Function
SW2	ROM write protect, ROMFS program select, bitrate selection
R1-R3, R6	Installed only for R6511Q/R6511AQ processors

For normal operation with standard ROM images, SW2 should have all switches set to the `OFF` position.

Console bitrate is selected with SW2 positions 3 and 4. The default configuration, with SW2 positions 3 and 4 off will provide a 4800 bps console with a 1 MHz system clock, or a 9600 bps console with a 2 MHz system clock. *Review notes in the following section concerning the selection of bitrates and potential error in higher speed rates.*

2.1 Configuring Console Speed

The address of the UART registers is fixed in the internal circuitry of the R65X1Q and cannot be changed. The UART bitrate is divided from the main system clock using one of the onboard counters. ROM images provided by Glitch Works, LLC use SW2 positions 3 and 4 to select the bitrate used for the ROM monitor or other startup routines. The following table describes the possible configurations available:

SW2-3	SW2-4	Clock	Console UART Speed
OFF	OFF	1 MHz	4800 bps
OFF	ON	1 MHz	2400 bps
ON	OFF	1 MHz	1200 bps
ON	ON	1 MHz	300 bps
OFF	OFF	2 MHz	9600 bps
OFF	ON	2 MHz	4800 bps
ON	OFF	2 MHz	2400 bps
ON	ON	2 MHz	600 bps

Note that while it is possible to set a division ratio for 9600 bps at 1 MHz (19200 bps at 2 MHz), *this division ratio will produce a bitrate clock with excessive deviation from standard frequencies.* Many terminals and other serial-connected devices will have problems with the error introduced at these bitrates; therefore, the SBC does not provide a user-configurable way to select them.

If a 9600 bps console UART speed is required, it is recommended that a 2 MHz system clock be used. While Rockwell only specs the A suffix R6501AQ and R6511AQ for 2 MHz operation, internal testing has shown good results with running non-A parts at 2 MHz. Operation is of course only guaranteed at Rockwell's published speeds.

Some serial equipment does not support operation at 4800 bps or operates unreliably at this speed. If you're experiencing problems with console output at 4800 bps, try selecting 2400 bps.

2.2 ROM Options

The R65X1Q SBC ROM occupies addresses `0xF000 - 0xFFFF`. ROM is addressed in 4K pages, with page control via Port C bits 0 through 2. Page control bits are set to `0x03` at reset and power-on. Port C bit 3 controls ROM enable; when set, ROM is enabled, when cleared, ROM is disabled. This bit is set at reset and power-on to allow ROM booting.

2.3 Processor Selection

Resistors R1 - R3 and R6 are installed only for R6511Q and R6511AQ processors, and are unnecessary for R6501Q and R6501AQ processors. These resistors provide pull-ups to I/O lines used on the SBC.

System clock frequency is determined by crystal Y1 and the internal division ratio of the R65X1Q processor. Consult the R6500 family datasheet for the processor in use to determine crystal frequency requirements.

2.4 Glitchbus Expansion

The R65X1Q SBC is expandable through a Glitchbus expansion header. Glitchbus is a generic 8-bit bus intended to be processor-agnostic. As implemented on the R65X1Q SBC, the Glitchbus can stack above or below the SBC using PC/104 style stacking headers. The R65X1Q SBC can also be used with right-angle headers and a Glitchbus backplane.

The Glitchbus includes signals for separate memory and I/O addressing, which the R65X1Q processors do not support. To enable the use of I/O mapped Glitchbus boards with the R65X1Q SBC, a 256 byte page of memory space from `0xEF00 - 0xEFFF` has been reserved as the Glitchbus I/O space.

3 Assembly

The R65X1Q SBC is designed to be easy to assemble for anyone with moderate soldering ability. It is a moderately complex board and will typically require between one and three hours of assembly time, depending on the skill of the assembler. The following tools will be required:

- Soldering iron, 20-40 W recommended, grounded tip
- Solder, 63/37 leaded solder recommended, Kester "44 Core" or similar
- Diagonal cutters or flush cutters
- Solder braid, solder sucker, or desoldering station, in the event errors are made
- Needle-nose pliers for bending component leads
- 1/4 and 1/8 W resistor lead forms (optional)

This manual does not cover basic soldering technique. If you are new to soldering, we recommend the Adafruit soldering guide and plenty of practice on a piece of protoboard before beginning assembly of this kit. The Adafruit guide can be found at:

`https://learn.adafruit.com/adafruit-guide-excellent-soldering`

3.1 Assembling the R65X1Q SBC

If you purchased a full Glitch Works parts kit, we recommend completing all assembly sections, since extra features can be disabled as needed. If supplying your own parts, you may choose which sections to complete based on the functionality required.

Note that pin 1 is designated with a square pad for all ICs, resistor packs, switches, and most connectors. Pin 1 is toward the top of the board, as seen from the front, for all ICs, switch packs, and radial electrolytic capacitors. The component (front) side of the board is the side which contains the white silkscreen legend. It is recommended to install components from shortest to tallest, which makes assembly without an assembly vise or jig easier, assuming the board is flipped over and soldered with the component side resting on a table top.

Some jumper headers and connector headers are press-fit and may require a bit of force or gentle wiggling to install. This is normal and helps keep the headers in place when the board is flipped over for soldering.

3.2 Assembly Checklist

- ☐ Verify parts list against kit contents or builder-provided parts
- ☐ Consult the assembly drawing for component locations and values
- ☐ Bend all 0.01 µF bypass capacitors (yellow axial bead) – position 2 on a 1/8 W lead form
- ☐ Install all 0.01 µF capacitors in positions marked C in assembly diagram
- ☐ Bend four 4.7 kΩ resistors and install in their marked locations – position 1 on a 1/4 W lead form
- ☐ If using a R6511Q or R6511AQ processor, hairpin bend four 4.7 kΩ resistors and set aside
- ☐ Install non-socketed DIP ICs at their marked locations. Do not install U1, U2, U3, U4, or U5
- ☐ Install a 16-pin socket at U1
- ☐ Install 28-pin sockets at U2, and U3
- ☐ Install the Rockwell processor at U4 – *sockets are not recommended for Rockwell QUIP package processors due to the force required for insertion and removal.* Note that QUIP package processors have a big notch at both ends, and a smaller off-center notch to indicate pin 1
- ☐ Install 33 µF 35 V capacitor at C19, bend leads with needle-node pliers
- ☐ Install micro tact pushbutton at SW1
- ☐ Install 22 pF radial ceramic capacitor at C10 and C11
- ☐ Install 10 nF radial ceramic capacitor at C3
- ☐ Install resistor pack at RP1
- ☐ Install DIP switch at SW2
- ☐ Install five 22 µF 16 V radial electrolytic capacitors at C4 - C8
- ☐ Install TO-92 DS1233 at U5
- ☐ If using a R6511Q or R6511AQ processor, install four previously hairpinned 4.7 kΩ resistors at R1 - R3, R6
- ☐ Install two 5x2 pin headers at J2, J3
- ☐ Install 2-pin Molex header at J4, observe orientation
- ☐ Install 5-pin Molex header at J1, observe orientation
- ☐ Install CPU clock crystal at Y1

3.3 Insert Socketed ICs

- ☐ Insert MAX232 level shifter into socket at U1
- ☐ Insert 28C256 EEPROM into socket at U2
- ☐ Insert SRAM into socket at U3

3.4 Assemble Console Cable

Do note that the R65X1Q SBC console port uses EIA RS-232 signalling levels, and is not compatible with USB TTL serial cables! If you are using a USB to serial cable, ensure that it uses EIA RS-232 levels before connecting it to the R65X1Q SBC.

Glitch Works parts kits include a DB25F connector for the R65X1Q SBC console cable, as well as a one-foot pigtail terminated in a 5-pin Molex KK-100 connector. This pigtail connects to J1, `CONSOLE`. Use the following table to build a console cable appropriate to your intended terminal:

J1 Pin	DB25F DCE Pin	DB25F DTE Pin	Function
1	5	4	Request to Send
2	3	2	Transmit Data
3	2	3	Receive Data
4	4	5	Clear to Send
5	7	7	Signal Ground

J1 pin 4 (`CTS`) and pin 1 (`RTS`) are not used in the standard R65X1Q SBC configuration. Console pigtails provided with Glitch Works parts kits omit both. These pins can be used if jumpered to other I/O pins for software control. Consult the schematic for more information.

A serial light box will help debug potential serial wiring problems, we highly recommend the addition of a light box to your toolkit if you regularly interface RS-232 equipment. Our personal favorite is the IQ Technologies SmartCable SC821 Plus.

3.5 Optional Glitchbus Expansion

The R65X1Q SBC may be expanded via Glitchbus. The SBC's form factor allows it to be used at any position in a stacked Glitchbus configuration. It may also be used with a right angle header and Glitchbus backplane. If using the R65X1Q SBC with a right angle header, *the header must be installed on the component side of the board.*

If used in a stacking configuration, the R65X1Q SBC can provide power to the Glitchbus stack through connector J4. Do not overload the pigtail or connector used for J4.

Right angle versions of J1 - J4 may be used, if desired. `RESET` switch SW1 may be a standard or right angle mini tact switch. This configuration is especially convenient when the R65X1Q SBC will be used in a Glitchbus stack, but will not be the topmost board.

4 Initial Checkout and Testing

Once the R65X1Q SBC is assembled, configure it as described in the "Configuration" section, starting on Page 2. Make sure that all positions on SW2 are open.

Double-check all ICs for proper orientation, check all solder joints for cold joints or solder bridges. Connect the power pigtail provided to a suitable regulated 5 V power supply capable of providing at least 500 mA. Connect your serial terminal or computer to the console port. Apply power to your system and press `RESET`. The eWoz sign-on message should be printed to the console, and eWoz should respond to appropriate user input.

For more information on the version of eWoz included with R65X1Q SBC kits, see:

`https://github.com/glitchwrks/ewoz_r6501`

4.1 Troubleshooting

If your R65X1Q SBC fails to come up, recheck all solder joints for cold joints, bridges, or missed pins – this is by far the most common problem we've observed during assembly workshops. Recheck configuration options. Ensure your serial terminal or terminal emulator software is properly configured and that your cable is wired correctly (a RS-232 light box is very helpful here).

Verify that `*BRESET` is properly strobing during power-up and when pressing the `RESET` button (SW1).

4.2 Repair and Service

If you purchased an assembled R65X1Q SBC from Glitch Works, LLC, your board is warranted to work on arrival. If you have assembled a kit that fails to work, you may return it to Glitch Works, LLC for evaluation, repair, and testing. For questions concerning returns or configuration, please visit `http://www.glitchwrks.com/` and click the "Contact" link.

Do note that while we will attempt to help those who have purchased used boards, there is no warranty extended.

5 Technical Notes

5.1 Port C and Board Control Register

The R65X1Q SBC uses a portion of the onboard Port C parallel I/O port (`0x0002`) as a board control register. Certain bits of Port C are used internally for "Full Address Mode," while others are used to control ROM operation. Port C is addressed at memory location `0x0002`. The bits of Port C are mapped as follows:

Port C Bit	Function	Notes
0	ROM Page Address, bit 0	Set on reset
1	ROM Page Address, bit 1	Set on reset
2	ROM Page Address, bit 2	Set on reset
3	ROM Disabled	Set (ROM enabled) on reset
4	Unused	
5	Unused	
6	Address Bus `A13`	Not user controllable
7	Address Bus `A14`	Not user controllable

Bits 0 through 2 control the selected 4K page of ROM available at `0xF000`. These bits are set on reset so that the last page of ROM is available for booting. Writing to these bits immediately changes the ROM page. Port C provides readback of these bits.

Bit 3 enables ROM when set, and disables ROM when clear. This allows unmapping ROM for use of system memory at `0xF000`. Writing a 0 to this bit clears it and immediately switches off ROM, writing a 1 to this bit switches ROM in. The selected ROM page is not affected. Bit 3 is set (ROM enabled) on reset. Its status can be read back through Port C.

Bits 4 and 5 are unused and can be jumpered to end user applications, if desired.

Bits 6 and 7 control address bus lines `A13` and `A14`, respectively. These bits are used in the "Full Address Mode" configuration of the R65X1Q processor, and are not available for user control as I/O pins. See the R6500 family datasheet relevant to the chosen processor for more information.

5.2 Port A and Switch Register

The low six bits of the onboard Port A parallel I/O port (`0x0000`) are mapped to the upper six positions of switch pack `SW1`. These bits are active high (a closed switch position reads as a binary 1). The upper two bits of Port C are used for the onboard UART and are not available as parallel I/O pins. The bits of Port A are mapped as follows:

Port A Bit	Function	Notes
0	PA0, SW2-8	ROMFS record, bit 0, closed reads 1
1	PA1, SW2-7	ROMFS record, bit 1, closed reads 1
2	PA2, SW2-6	ROMFS record, bit 2, closed reads 1
3	PA3, SW2-5	ROMFS record, bit 3, closed reads 1
4	PA4, SW2-4	Bitrate selection, closed reads 1
5	PA5, SW2-3	Bitrate selection, closed reads 1
6	UART Transmit Data	
7	UART Receive Data	

Bits 0 through 5 reflect the state of SW2 positions 8 through 3. A 1 in a given bit position corresponds to a closed switch. These positions are labeled `PA0 - PA5` in the silkscreen. `PA0 - PA3` can be used by Glitch Works software to select the ROMFS record to load into memory at reset. `PA4 - PA5` are used by Glitch Works software to set the console UART bitrate, as described in Section 2.1, "Configuring Console Speed."

Bits 6 and 7 are used by the R65X1Q internal UART and are not available as parallel I/O pins.

5.3 Memory Map

The R65X1Q SBC operates in "Full Address Mode" and has the following memory map:

Address Range	Contents
`0x0000 - 0x0003`	Parallel I/O ports
`0x0004 - 0x000F`	Reserved (not usable)
`0x0010 - 0x001F`	R65X1Q control registers
`0x0020 - 0x003F`	Reserved (not usable)
`0x0040 - 0x00FF`	R65X1Q internal RAM
`0x0100 - 0x7FFF`	Static RAM, IC socket U3
`0x8000 - 0xEEFF`	Glitchbus expansion memory space
`0xEF00 - 0xEFFF`	Glitchbus expansion I/O space
`0xFF00 - 0xFFFF`	Glitchbus expansion memory space, when ROM is disabled
`0xFF00 - 0xFFFF`	4K page of ROM, IC socket U2, when ROM is enabled

Memory occupied by the static RAM in socket U2 may be overlaid by external devices on the Glitchbus using the `*BMASK` signal.

Consult the Rockwell R6500 family datasheet specific to the processor in use for more information about onboard I/O and memory devices.

6 Errata and Clarifications

6.1 ROM Compatibility

The ROM socket at U2 is compatible with JEDEC standard 32K x 8 static RAM, Ferroelectric RAM (FeRAM), and 28C256 EEPROMs. It may not be compatible with some manufacturers' UV EPROMs, such as the common 27256 EPROM.

7 Parts List

If you purchased a full Glitch Works parts kit, be sure it includes the following:

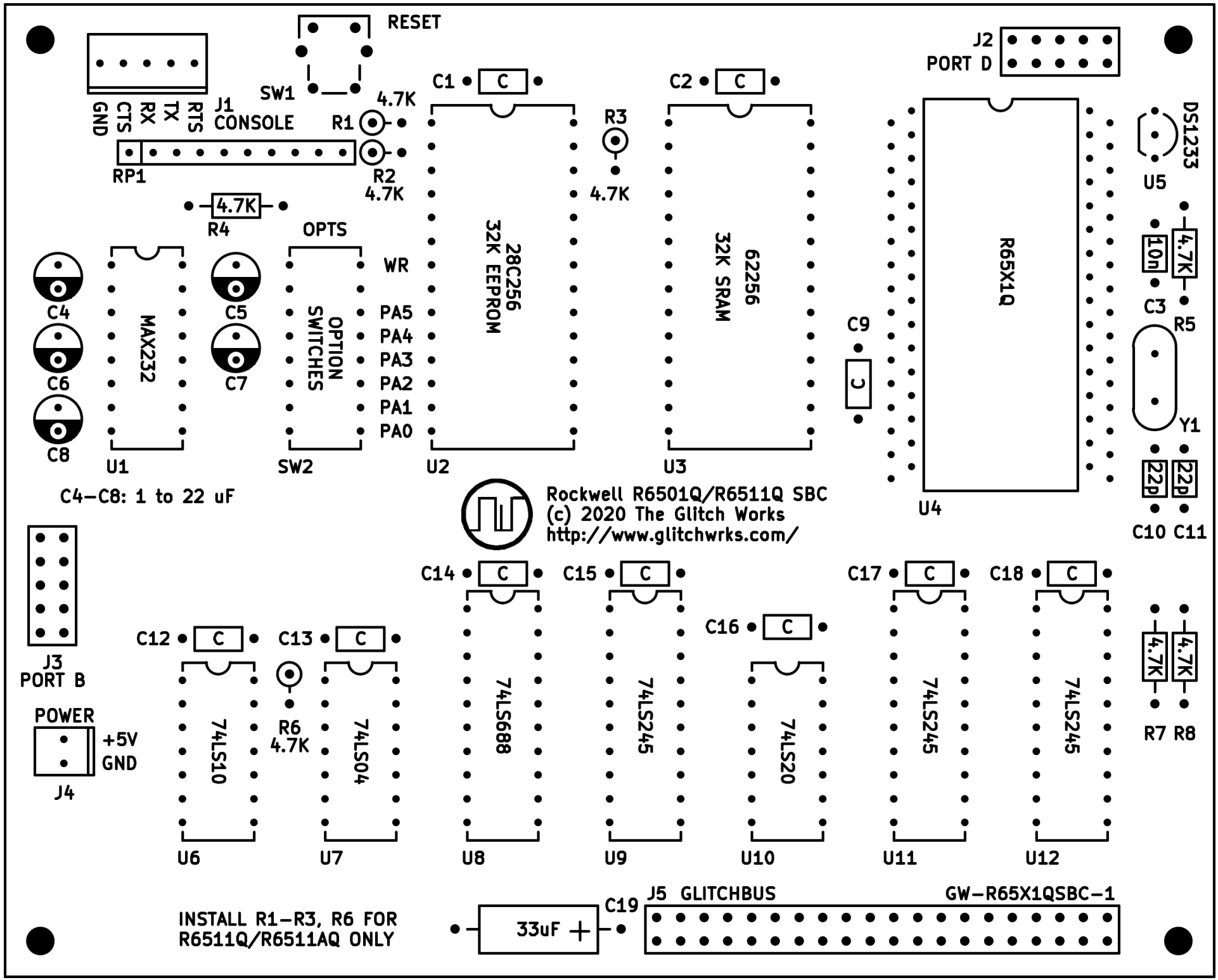
- ☐ 2x 22 pF radial ceramic capacitor
- ☐ 10x 0.01 µF axial ceramic capacitor (yellow bead)
- ☐ 1x 10 nF 16 V radial ceramic capacitor
- ☐ 1x 33 µF 35 V axial electrolytic capacitor
- ☐ 5x 22 µF 16 V radial electrolytic capacitor
- ☐ 4x 4.7 kΩ 1/4 W resistor (see above note)
- ☐ 1x 220 Ω x 9 SIP resistor packs (see note above)
- ☐ 1x 4 MHz crystal
- ☐ 1x Rockwell R6501Q CPU
- ☐ 1x 28C256 EEPROM, preloaded with R65X1Q SBC firmware
- ☐ 1x JEDEC 62256-type 32K x 8 static RAM
- ☐ 1x 74LS04 hex inverter
- ☐ 1x 74LS10 triple 3-input NAND gate
- ☐ 1x 74LS20 dual 4-input NAND gate
- ☐ 3x 74LS245 transceiver
- ☐ 1x 74LS688 magnitude comparator
- ☐ 1x MAX232 RS-232 level shifter
- ☐ 1x DS1233 EconoReset
- ☐ 1x 8-position DIP switch
- ☐ 1x mini tact pushbutton switch
- ☐ 2x 5x2-pin headers
- ☐ 1x 2-position Molex KK-100 header
- ☐ 1x 5-position Molex KK-100 header
- ☐ 2x 28-pin IC socket
- ☐ 1x 16-pin IC socket
- ☐ 1x Power pigtail
- ☐ 1x RS-232 console pigtail
- ☐ 1x DB25F connector

7.1 Substitutions

The following substitutions may be made if you have purchased a bare board and are supplying your own parts, or in a full Glitch Works parts kit:

- Any compatible 7400 series family logic ICs may be used (for example, a 74LS04 in the parts list may be shipped as a 7404, 74S04, 74F04, 74LS04, 74ALS04, or 74HCT04)
- All 4.7 kΩ resistors on the GW-R65X1QSBC-1 are pull-up or pull-down resistors, and may be any value from 2.2 kΩ to 10 kΩ, even though they are indicated as 4.7 kΩ on the assembly drawing
- Resistors may be of varying precision and body type

Additionally, see Section 2.3, "Processor Selection" for information on choosing a processor and crystal combination for user-supplied parts.


RESET
SW1
J1
CONSOLE
GND
CTS
RX
TX
RTS
RP1
R1
R2
4.7K
R3
4.7K
R4
4.7K
OPTS
WR
PA5
PA4
PA3
PA2
PA1
PA0
SW2
OPTION SWITCHES
C1
C2
C
28C256
32K EEPROM
62256
32K SRAM
U1
MAX232
U2
U3
C4
C5
C6
C7
C8
C4–C8: 1 to 22 uF
J2
PORT D
R65X1Q
U4
C9
DS1233
U5
10n
C3
Y1
22p
C10
C11
R5
Rockwell R6501Q/R6511Q SBC
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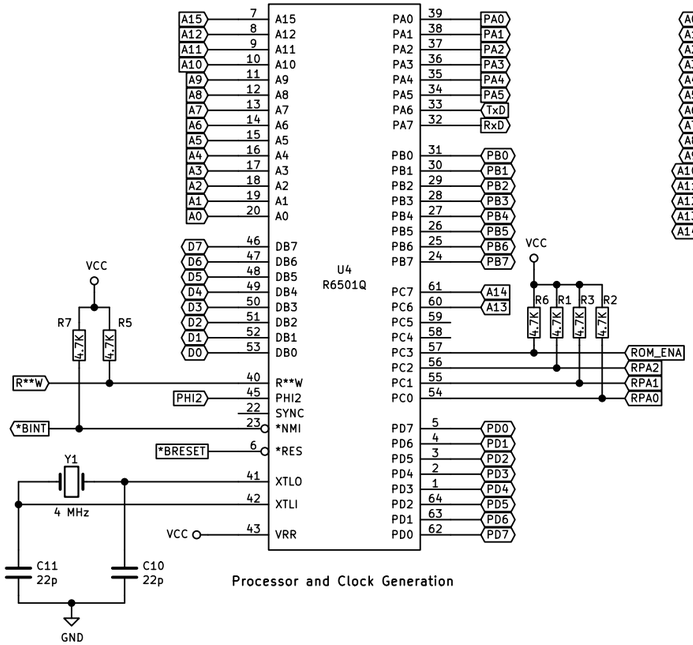
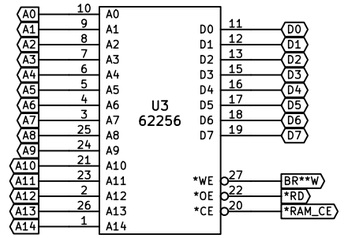
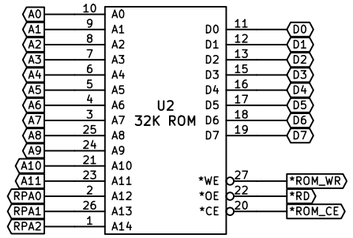
J3
PORT B
POWER
+5V
GND
J4
C12
C13
C14
C15
C16
C17
C18
74LS10
74LS04
74LS688
74LS245
74LS20
74LS245
74LS245
U6
U7
U8
U9
U10
U11
U12
R6
4.7K
R7
R8
INSTALL R1–R3, R6 FOR
R6511Q/R6511AQ ONLY
C19
33uF
J5 GLITCHBUS
GW–R65X1QSBC–1



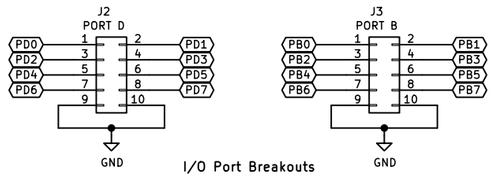
Processor and Clock Generation



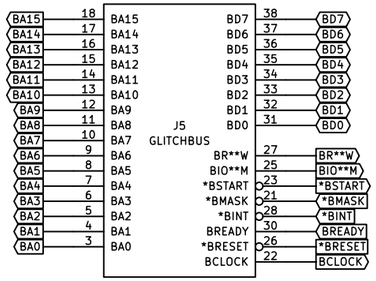
External RAM 0x0000 – 0x7FFF



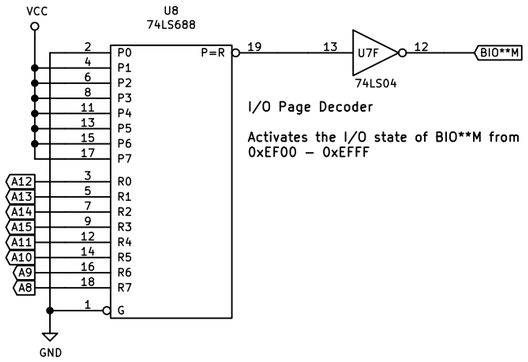
EEPROM 0xF000 – 0xFFFF
Available in 4K segments



I/O Port Breakouts

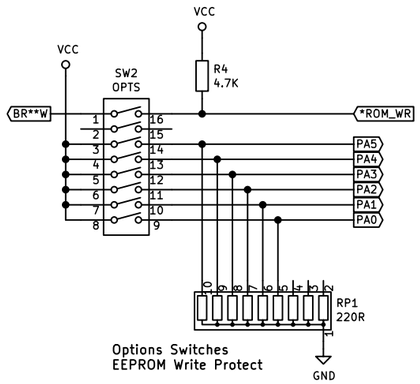


Glitchbus Expansion Connector

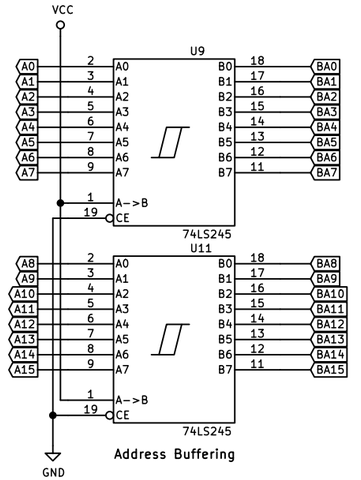


I/O Page Decoder

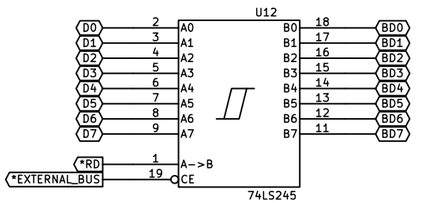
Activates the I/O state of BIO**M from
0xEF00 – 0xEFFF



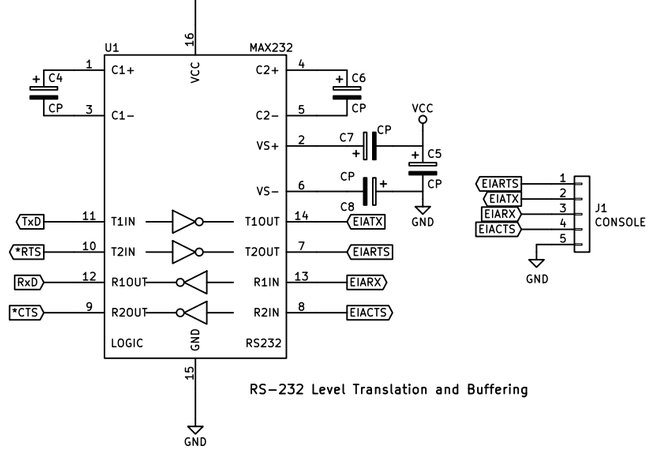
Options Switches
EEPROM Write Protect



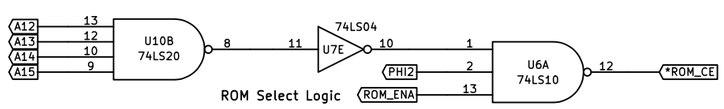
Address Buffering



Data Buffer

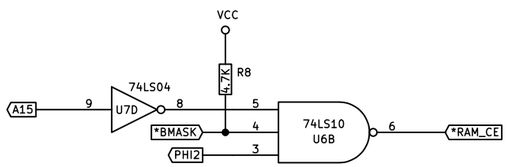


RS–232 Level Translation and Buffering

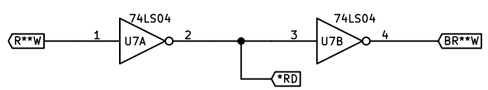


ROM Select Logic

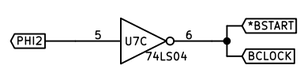
Places 4K segment of EEPROM at 0xF000



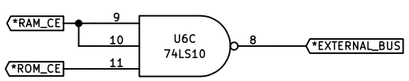
External RAM Select Logic



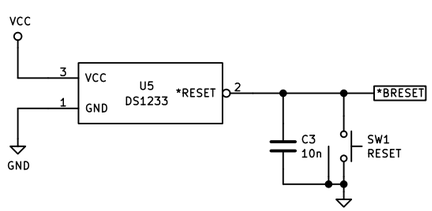
*RD and BR**W Generator and Buffer



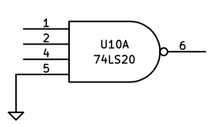
*BSTART Generator and Clock Buffer



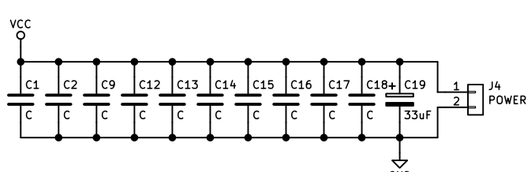
External Bus Control



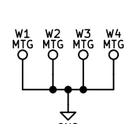
Power–On Reset and Supervisor



Spare Gates



Decoupling and Bypass



Mounting Holes

GW–R65X1QSBC–1
J. Chapman
Glitch Works, LLC
Sheet: /
File: gw–r65x1qsbc–1.sch

Title: R65X1Q Single Board Computer

Size: USLedger	Date: 2020–09–28	**Rev: 2**
KiCad E.D.A. kicad 5.1.2		Id: 1/1