BUS DEFINITIONS

PIN NO.	SYMBOL	NAME	FUNCTION
1	+8V	+8 Volts	Unregulated voltage on bus, supplied to PC boards and regulated to 5V.
2	+18V	+18 Volts	Positive preregulated voltage.
3	XRDY	EXTERNAL READY	External ready input to CPU board's ready circuitry.
4	VI0	Vectored Interrupt Line #0	
5	VI1	Vectored Interrupt Line #1	
6	VI2	Vectored Interrupt Line #2	
7	VI3	Vectored Interrupt Line #3	
8	VI4	Vectored Interrupt Line #4	
9	VI5	Vectored Interrupt Line #5	
10	VI6	Vectored Interrupt Line #6	
11	VI7	Vectored Interrupt #7	
12 to 17			TO BE DEFINED
18	$\overline{\text{STAT DSB}}$	$\overline{\text{STATUS DISABLE}}$	Allows the buffers for the 8 status lines to be tri-stated.
19	$\overline{\text{C/C DSB}}$	$\overline{\text{COMMAND/CONTROL DISABLE}}$	Allows the buffers for the 6 output command/control lines to be tri-stated.
20*	UNPROT	UNPROTECT	Input to the memory protect flip-flop on a given memory board.
21	SS	SINGLE STEP	Indicates that the machine is in the process of performing a single step (i.e., that SS flip-flop on D/C is set).
22	$\overline{\text{ADD DSB}}$	$\overline{\text{ADDRESS DISABLE}}$	Allows the buffers for the 16 address lines to be tri-stated.
23	$\overline{\text{DO DSB}}$	$\overline{\text{DATA OUT DISABLE}}$	Allows the buffers for the 8 data output lines to be tri-stated.
24	Ø2	PHASE 2 CLOCK	
25	Ø1	PHASE 1 CLOCK	

* Jump to ground on BYT-8 motherboard.

PIN NO.	SYMBOL	NAME	FUNCTION
26	PHLDA	HOLD ACKNOWLEDGE	Processor command/control output signal that appears in response to the HOLD signal; indicates that the data and address bus will go to the high impedance state and processor will enter HOLD state after completion of the current machine cycle.
27	PWAIT	WAIT	Processor command/control signal that appears in response to the READY signal going low; indicates processor will enter a series of .5 microsecond WAIT states until READY again goes high.
28	PINTE	INTERRUPT ENABLE	Processor command/control output signal; indicates interrupts are enabled, as determined by the contents of the CPU internal interrupt flip-flop. When the flip-flop is set (Enable Interrupt instruction), interrupts are accepted by the CPU; when it is reset (Disable Interrupt instruction), interrupts are inhibited.
29	A5	Address Line #5	
30	A4	Address Line #4	
31	A3	Address Line #3	
32	A15	Address Line #15	(MSB)
33	A12	Address Line #12	
34	A9	Address Line #9	
35	DO1	Data Out Line #1	
36	DO0	Data Out Line #0	(LSB)
37	A10	Address Line #10	
38	DO4	Data Out Line #4	
39	DO5	Data Out Line #5	
40	DO6	Data Out Line #6	
41	DI2	Data In Line #2	
42	DI3	Data In Line #3	
43	DI7	Data In Line #7	(MSB)
44	SM1	MACHINE CYCLE 1	Status output signal that indicates that the processor is in the fetch cycle for the first byte of an instruction.
45	SOUT	OUTPUT	Status output signal that indicates the address bus contains the address of an output device and the data bus will contain the output data when $\overline{PWR}$ is active.

PIN NO.	SYMBOL	NAME	FUNCTION
46	SINP	INPUT	Status output signal that indicates the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active.
47	SMEMR	MEMORY READ	Status output signal that indicates the data bus will be used to read memory data.
48	SHLTA	HALT	Status output signal that acknowledges a HALT instruction.
49	$\overline{\text{CLOCK}}$	$\overline{\text{CLOCK}}$	Inverted output of the Ø2 CLOCK.
50	GND	GROUND	
51	+8V	+8 Volts	Unregulated input to 5 volt regulators.
52	-18V	-18 Volts	Negative preregulated voltage.
53	$\overline{\text{SSWI}}$	$\overline{\text{SENSE SWITCH INPUT}}$	Indicates that an input data transfer from the sense switches is to take place. This signal is used by the Display/ Control logic to: a) Enable sense switch drivers. b) Enable the Display/Control Board drivers Data Input (FDIØ-FD17). c) Disable the CPU Board Data Input Drivers (DIØ-D17).
54	$\overline{\text{EXT CLR}}$	$\overline{\text{EXTERNAL CLEAR}}$	Clear signal for I/O devices (front panel switch closure to ground).
*GRD 55	RTC	REAL TIME CLOCK	60HZ signal used as timing reference by the Real Time Clock/Vectored Interrupt Board.
56 to 67	PHANTOM		TO BE DEFINED
68	MWRITE	MEMORY WRITE	Indicates that the data present on the Data Out Bus is to be written into the memory location currently on the address bus.
69	$\overline{\text{PS}}$	$\overline{\text{PROTECT STATUS}}$	Indicates the status of the memory protect flip-flop on the memory board currently addressed.
70*	PROT	PROTECT	Input to the memory protect flip-flop on the memory board currently addressed.

* Jump to ground on BYT-8 motherboard.

PIN NO.	SYMBOL	NAME	FUNCTION
71	RUN	RUN	Indicates that the STOP/RUN flip-flop is reset; i.e., machine is in RUN mode.
72	PRDY	PROCESSOR READY	Memory and I/O input to the CPU board wait circuitry.
73	$\overline{\text{PINT}}$	$\overline{\text{INTERRUPT REQUEST}}$	The processory recognizes an interrupt request on this line at the end of the current instruction or while halted. If the processor is in the HOLD state or the Interrupt Enable flip-flop is reset, it will not honor the request.
74	$\overline{\text{PHOLD}}$	$\overline{\text{HOLD}}$	Processor command/control input signal that requests the processor enter the HOLD state; allows an external device to gain control of address and data buses as soon as the processor has completed its use of these buses for the current machine cycle.
75	$\overline{\text{PRESET}}$	$\overline{\text{RESET}}$	Processor command/control input; while activated, the content of the program counter is cleared and the instruction register is set to 0.
76	PSYNC	SYNC	Processor command/control output; provides a signal to indicate the beginning of each machine cycle.
77	$\overline{\text{PWR}}$	$\overline{\text{WRITE}}$	Processor command/control output; used for memory write or I/O output control. Data on the data bus is stable while the $\overline{\text{PWR}}$ is active.
78	PDBIN	DATA BUS IN	Processor command/control output; indicates to external circuits that the data bus is in the input mode.
79	A0	Address Line #0	(LSB)
80	A1	Address Line #1	
81	A2	Address Line #2	
82	A6	Address Line #6	
83	A7	Address Line #7	
84	A8	Address Line #8	
85	A13	Address Line #13	
86	A14	Address Line #14	
87	A11	Address Line #11	
88	DO2	Data Out Line #2	
89	DO3	Data Out Line #3	
90	DO7	Data Out Line #7	

PIN NO.	SYMBOL	NAME	FUNCTION
91	DI4	Data In Line #4	
92	DI5	Data In Line #5	
93	DI6	Data In Line #6	
94	DI1	Data In Line #1	
95	DI0	Data In Line #0	(LSB)
96	SINTA	INTERRUPT ACKNOWLEDGE	Status output signal; acknowledges signal for INTERRUPT request.
97	$\overline{\text{SWO}}$	$\overline{\text{WRITE OUT}}$	Status output signal; indicates that the operation in the current machine cycle will be a WRITE memory or output function.
98	SSTACK	STACK	Status output signal indicates that the address bus holds the pushdown stack address from the Stack Pointer.
99	$\overline{\text{POC}}$	$\overline{\text{POWER-ON CLEAR}}$	
100	GND	GROUND	