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\*\*\*\*\* S-100 COMPUTER PRODUCTS 32K STATIC RAM ASSEMBLY \*\*\*\*\*  
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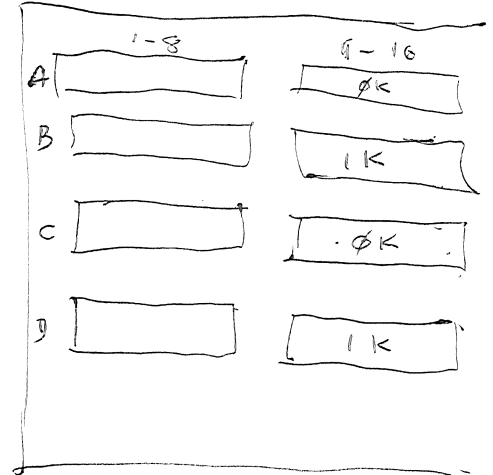
NOTE : ALL COMPONENTS ARE PLACED ON THE SIDE OF THE BOARD WITH THE WHITE LEGENDS. ALL SOLDERING IS DONE ON THE SIDE OF THE BOARD WITHOUT THE WHITE LEGENDS.

NOTE : WHEN INSTALLING INTEGRATED CIRCUITS AND SOCKETS OBSERVE THAT PIN 1 ON THE I. C. PADS ON THE BOARD IS SQUARE. ORIENT THE PARTS PROPERLY.

1. INSTALL 64 18-PIN SOCKETS AT LOCATIONS A1 THRU A16, B1 THRU B16, C1 THRU C16, AND D1 THRU D16.
2. INSTALL 11 16-PIN SOCKETS AT LOCATIONS C17, C18, C19, D17, D18, E1, E2, E3, E4, E5, AND E6.
3. INSTALL 1 14-PIN SOCKET AT LOCATION D19.
4. INSTALL 1 DIPPED TANTALUM CAPACITOR C35 WITH THE LEAD WITH THE DOT OR PAINT STRIPE ADJACENT INSERTED INTO THE HOLE MARKED (+).
5. INSTALL 37 .1UFD OR .05UFD CERAMIC DISC CAPACITORS AT THE LOCATIONS SHOWN ON THE LEGEND.
6. THERE ARE TWO DIFFERENT PINOUTS OF 1K X 4 STATIC RAM CHIPS. IF YOUR KIT WAS SUPPLIED WITH MEMORY CHIPS MARKED '2114' OR '4045' PERFORM STEP 8. IF YOUR MEMORY CHIPS ARE MARKED 'AMD 9135' PERFORM STEP 7.
7. INSTALL 8 JUMPERS IN THE AREAS TO THE RIGHT OF THE MEMORY ARRAY AS FOLLOWS : 14 TO A8, 13 TO A9, 6 TO D4, 7 TO D5, 14 TO A8, 13 TO A9, 6 TO D0, 7 TO D1. PROCEED TO STEP 9.
8. INSTALL 8 JUMPERS IN THE AREAS TO THE RIGHT OF THE MEMORY ARRAY AS FOLLOWS : 14 TO D4, 13 TO D5, 6 TO A8, 7 TO A9, 14 TO D0, 13 TO D1, 6 TO A8, 7 TO A9.
9. INSTALL THE LARGE RESISTOR R1.
10. INSTALL THE HEATSINK USING 4 SETS OF #4 BOLTS, LOCKWASHERS, AND NUTS.
1. INSTALL THE 2N6132 PASS TRANSISTOR AND INSULATOR IN THE UPPER AREA OF THE HEATSINK. INSTALL THE 7805 OR LM340-5 IN THE LOWER AREA OF THE HEATSINK. SECURE THE 2N6132 AND 7805 OR LM340-5 WITH #4 HARDWARE AS BEFORE. TIGHTEN ALL NUTS.
2. CHECK ALL SOLDERING FOR COLD CONNECTIONS. CHECK FOR SHORTED +5VDC SUPPLY BY CHECKING RESISTANCE BETWEEN PIN 9 AND PIN 18 ON ANY MEMORY SOCKET. THE READING SHOULD BE GREATER THAN 200 OHMS. IF NOT CHECK THAT THE 2N6132 AND 7805 OR LM340-5 LEADS ARE NOT TOUCHING THE HEATSINK AND THAT NO SOLDER BRIDGES EXIST. IF YOU CANNOT OBTAIN THE PROPER READING CONTACT YOUR DEALER. DO NOT APPLY POWER UNLESS THE PROPER READING IS OBTAINED!!!
3. INSTALL INTEGRATED CIRCUITS AS FOLLOWS : 4 74LS138 AT LOCATIONS E1, E2, E4, AND E6, 1 4009 AT LOCATION E5, 1 4010 AT LOCATION E3, 3 74367 AT LOCATIONS C17, C18, AND C19, 2 74368 AT LOCATIONS D17, AND D18, 1 7400 AT LOCATION D19.

14. INSTALL MEMORY CHIPS AT THE LOCATIONS DESIRED.

STARTING ADDR. (10)	STARTING ADDR. (16)	BIT 7-4 LOCATION	BIT 3-0 LOCATION
0	0000	A9	C9
1024	0400	B9	D9
2048	0800	A10	C10
3072	0C00	B10	D10
4096	1000	A11	C11
5120	1400	B11	D11
6144	1800	A12	C12
7168	1C00	B12	D12
8192	2000	A13	C13
9216	2400	B13	D13
10240	2800	A14	C14
11264	2C00	<del>E14</del>	D14
12288	3000	A15	C15
13312	3400	B15	D15
14336	3800	A16	C16
15360	3C00	B16	D16
16384	4000	A1	C1
17408	4400	B1	D1
18432	4800	A2	C2
19456	4C00	B2	D2
20480	5000	A3	C3
21504	5400	B3	D3
22528	5800	A4	C4
23552	5C00	B4	D4
24576	6000	A5	C5
25600	6400	B5	D5
26624	6800	A6	C6
27648	6C00	B6	D6
28672	7000	A7	C7
29696	7400	B7	D7
30720	7800	A8	C8
31744	7C00	B8	D8

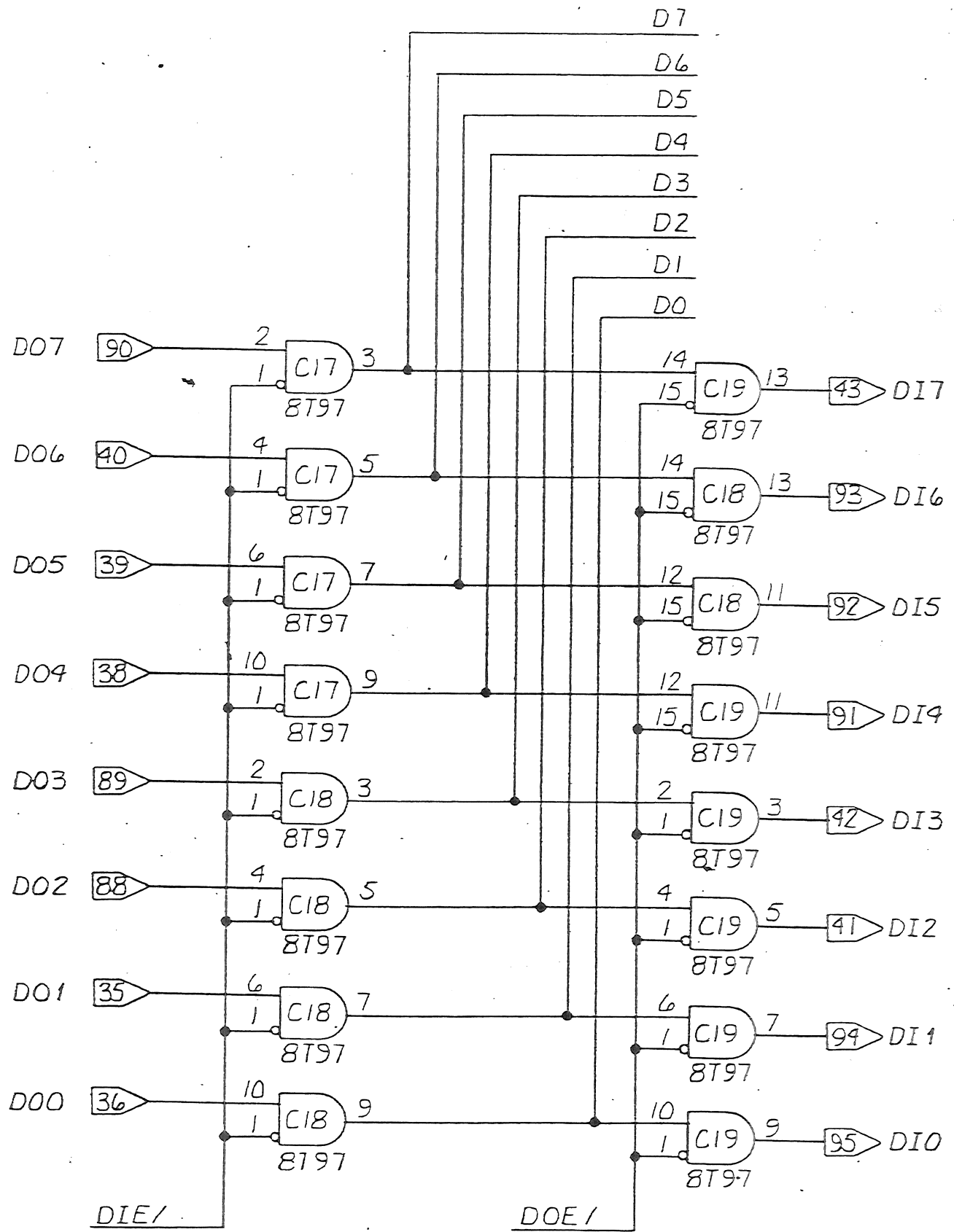


15. IF THIS BOARD IS TO OCCUPY THE TOP 32K OF ADDRESS SPACE, IN THE PAD AREA ADJACENT TO THE EDGE CONNECTOR, CUT THE ETCH FROM S2 TO S3 AND JUMPER S1 TO S2. IF THE SYSTEM CONTAINS A DMA CONTROLLER WHICH DOES NOT GENERATE PSYNC, REMOVE THE 7400 AT D19, BEND OUT PIN 1 SO THAT IT WILL NOT MAKE CONTACT AND REINSTALL.

16. END OF ASSEMBLY.

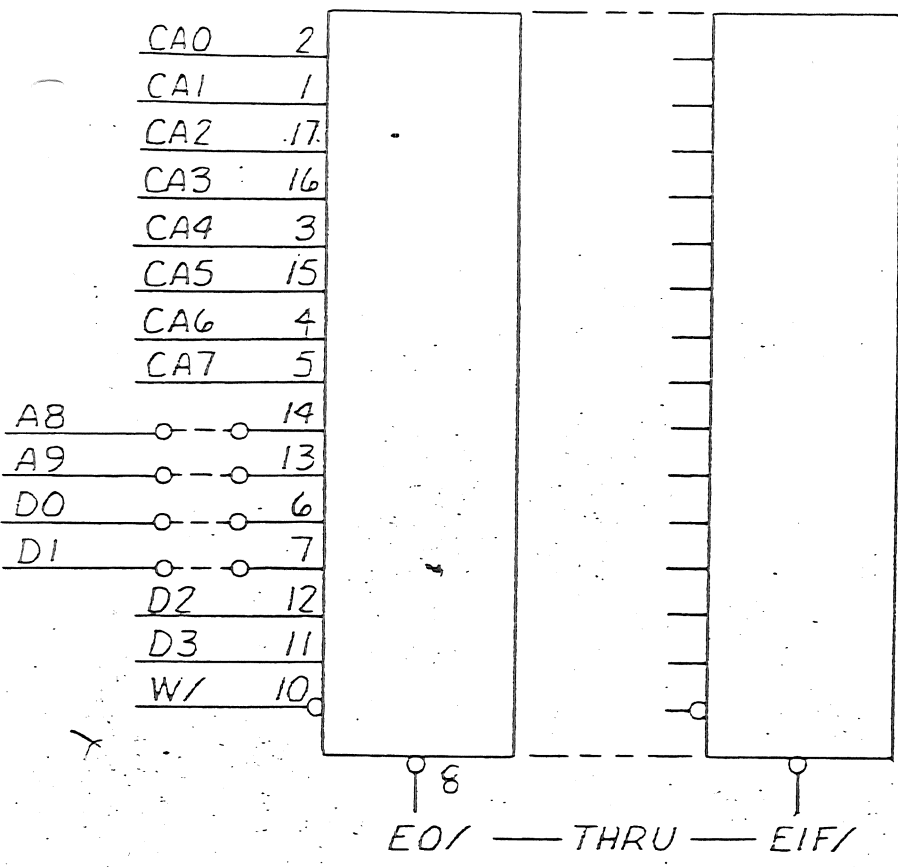
CONTROL CHECKS - WITH AN OSCILLISCOPE OR VOM MEASURE +5VDC BETWEEN PIN 18(+5VDC) AND PIN 9(GND) ON ANY MEMORY CHIP. THE MEASURED VALUE SHOULD BE BETWEEN +4.5VDC AND +5.5VDC. TURN OFF SYSTEM AND REMOVE THE 74367 I.C.'S AT C18 AND C19. REMOVE ALL OTHER SYSTEM MEMORY BOARDS. TURN ON SYSTEM AND RESET. WITH A LOGIC PROBE OR OSCILLISCOPE CHECK FOR PULSE TRAINS AT D19 PIN 3, D19 PIN 8, D18 PIN 11, C17 PIN 11, C17 PIN 13, D17 PIN 9, D17 PIN 7, D17 PIN 11, D17 PIN 5, D18 PIN 5, D17 PIN 3, D18 PIN 3, D17 PIN 13, E4 PINS 15, 14, 13, 12, 11, 10, 9, AND 7, E6 PINS 15, 14, 13, 12, 11, 10, 9, AND 7, E1 PINS 15, 14, 13, 12, 11, 10, 9, AND 7, E2 PINS 15, 14, 13, 12, 11, 10, 9, AND 7. IF ANY ERRORS HAVE BEEN DETECTED UTILIZE THE LOGIC DIAGRAM TO ISOLATE THE FAULT. THIS ENDS THE CONTROL SECTION CHECKOUT. TURN OFF SYSTEM AND REINSTALL 74367 I.C.'S AT LOCATIONS C18 AND C19. TURN ON SYSTEM.

2. DATA SECTION CHECKS - IF A SINGLE BIT ERROR OCCURS AT ALL ADDRESSES TURN OFF THE SYSTEM AND EXCHANGE THE 74367 I.C.'S AT LOCATION C17 AND C19. TURN ON SYSTEM. IF THE ERRONEOUS BIT MOVED INTO BITS 3 THRU 8 THEN REPLACE THE 74367 I.C. AT LOCATION C19. IF THE ERRONEOUS BIT MOVED INTO BITS 7 THRU 4 THEN REPLACE THE 74367 I.C. AT LOCATION C17. IF THE ERRONEOUS BIT DID NOT MOVE REPLACE THE 74367 I.C. AT LOCATION C18. IF DATA ERRORS OCCUR AT A SINGLE ADDRESS OR AT A GROUP OF ADDRESSES THEN ISOLATE THE RESPONSIBLE MEMORY CHIP USING THE TABLE IN THE ASSEMBLY SECTION BEFORE RETURNING A SUSPECTED BAD MEMORY CHIP ENSURE THAT THE MEMORY CHIP IS CORRECTLY SEATED IN ITS SOCKET. IF ANY ERRORS STILL EXIST CALL YOUR DEALER.

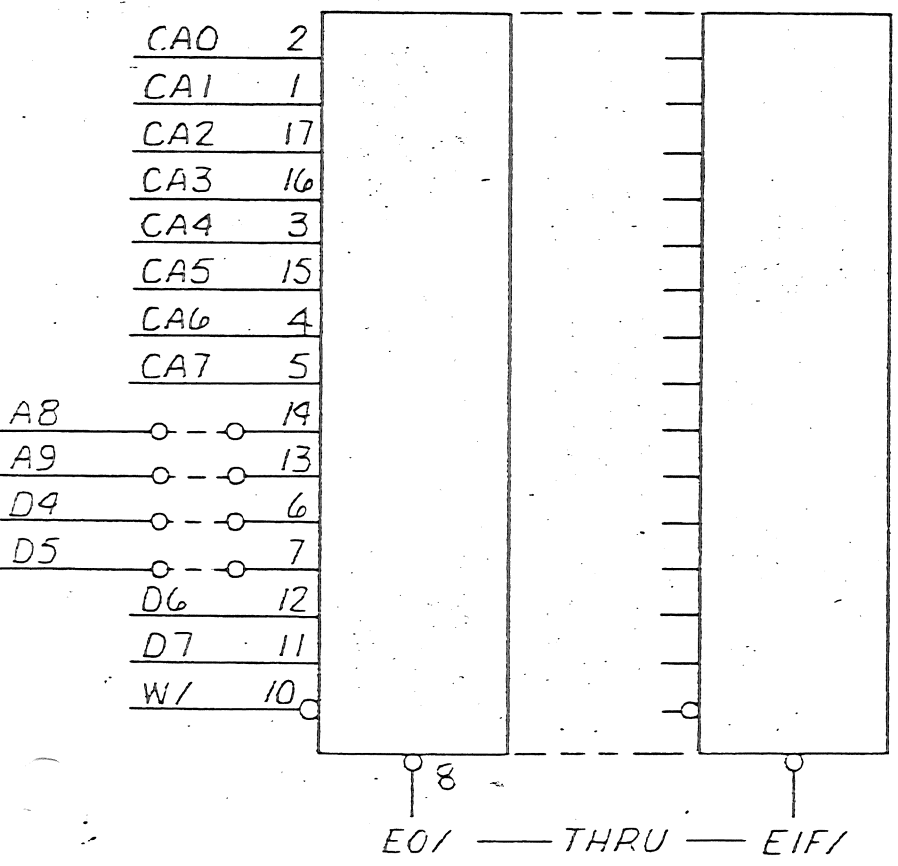


\* {  
 A8  
 A9  
 D0  
 D1

\* {  
 A8  
 A9  
 D4  
 D5

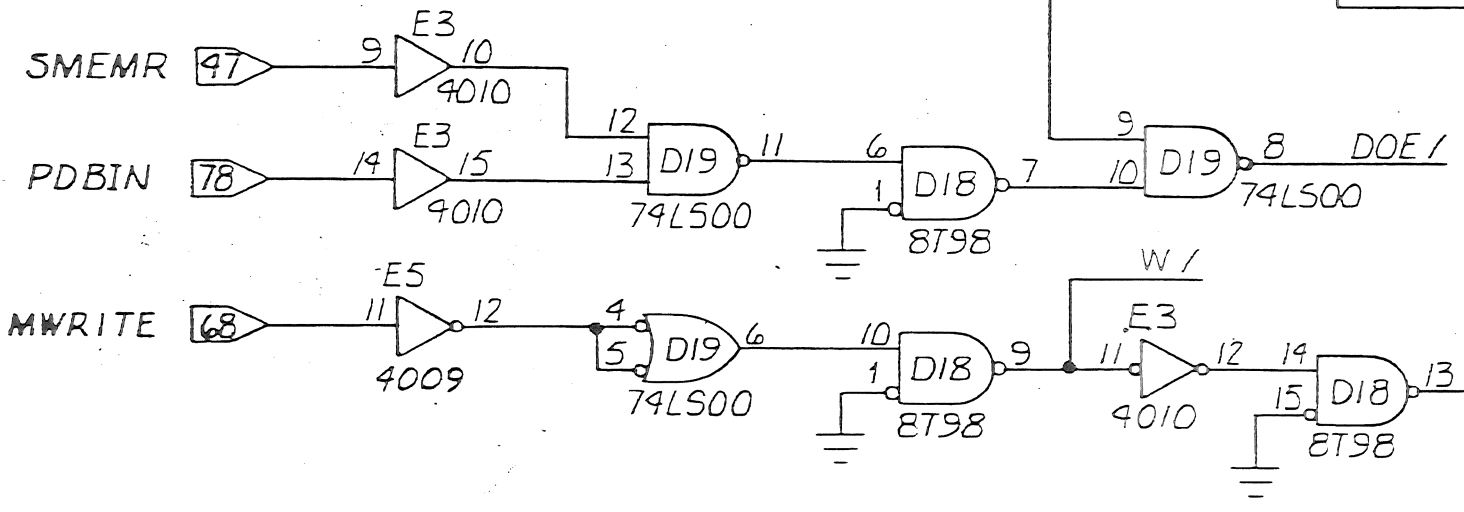
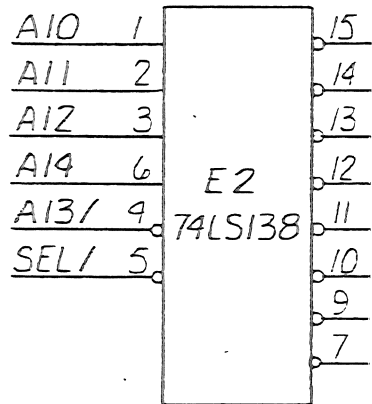
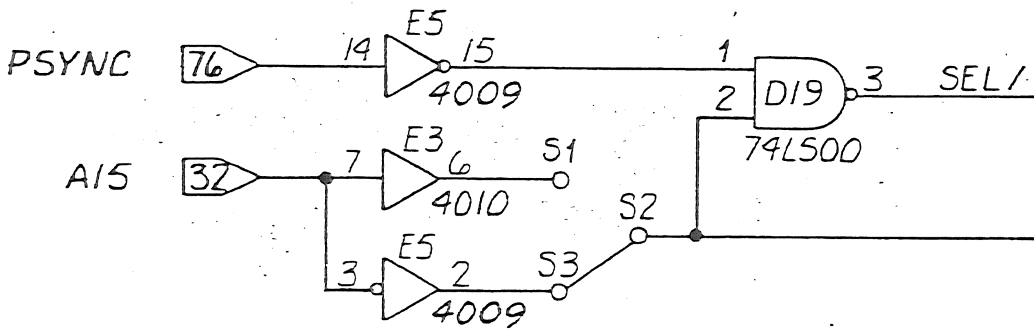
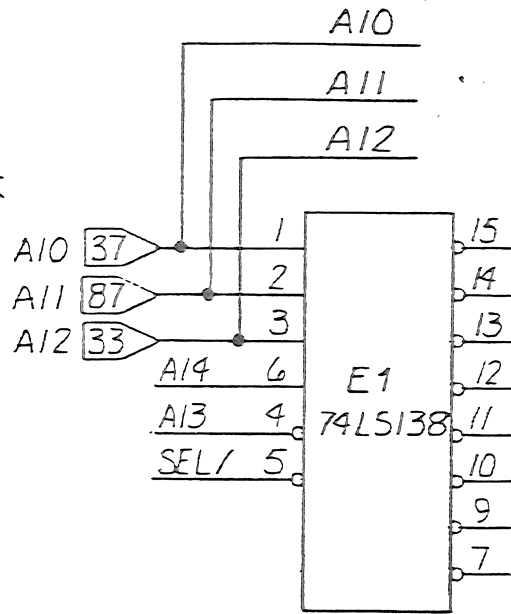
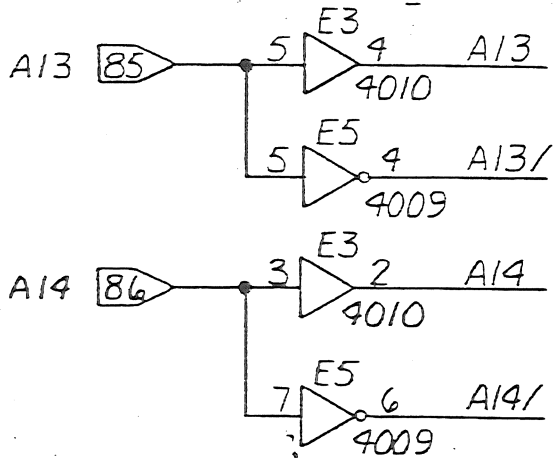
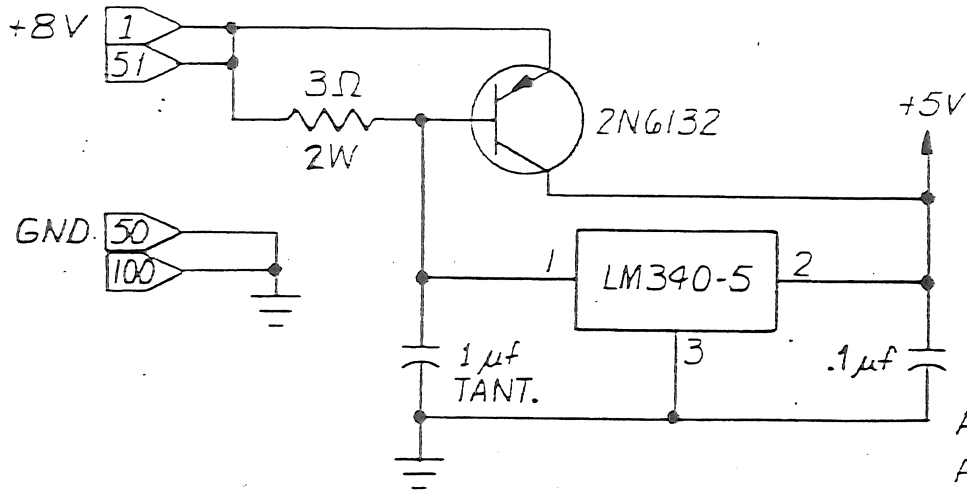


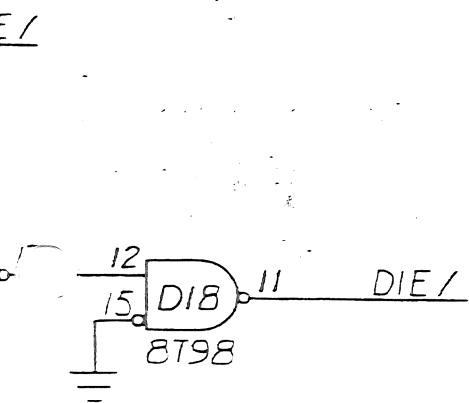
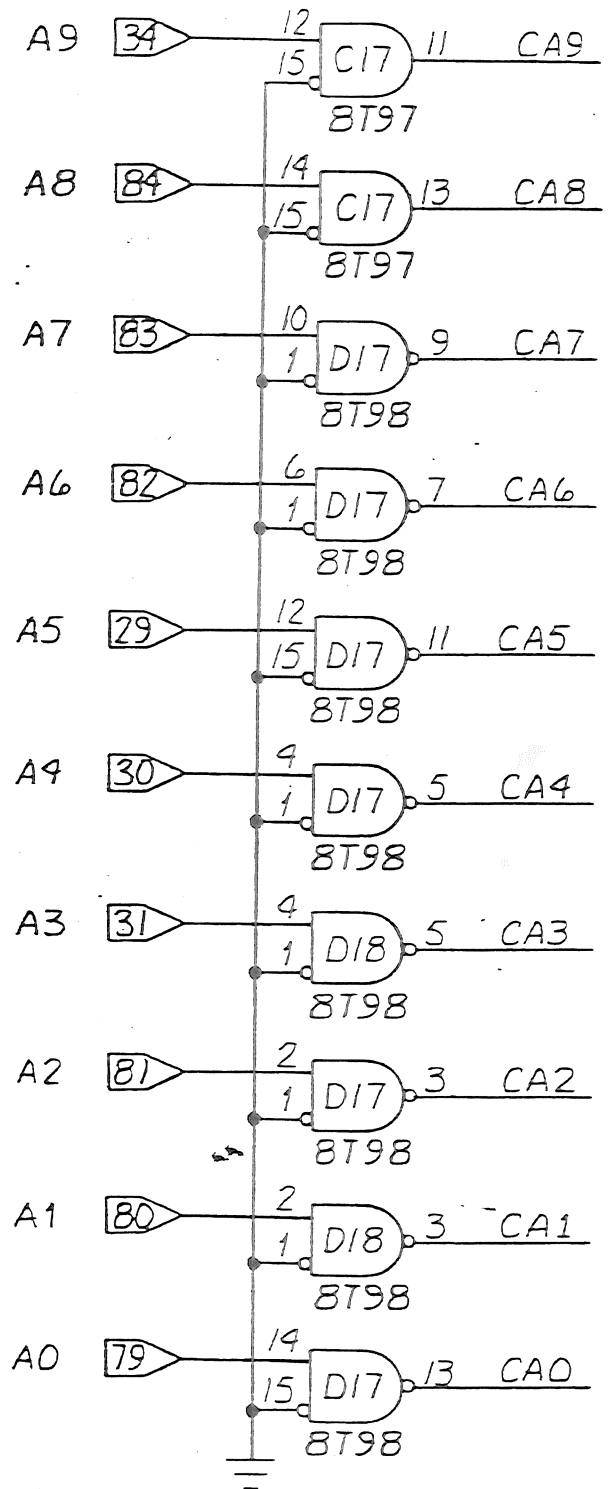
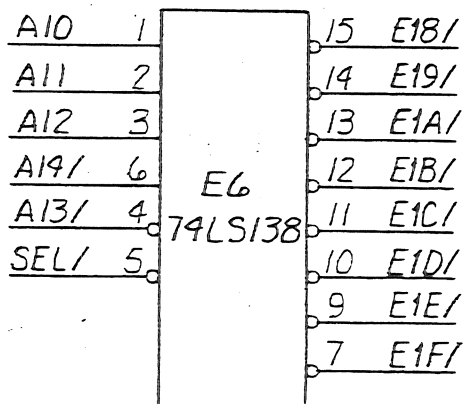
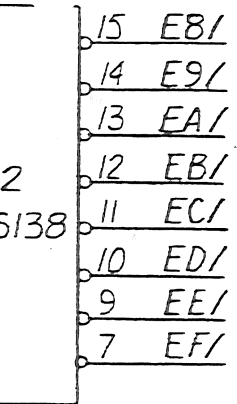
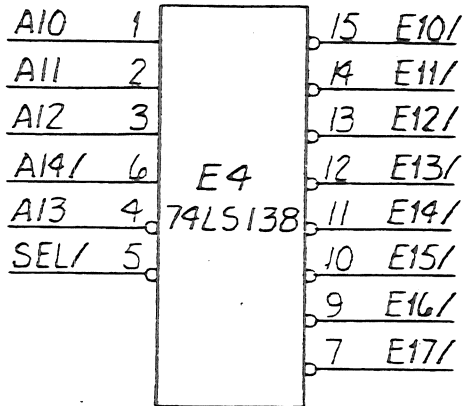
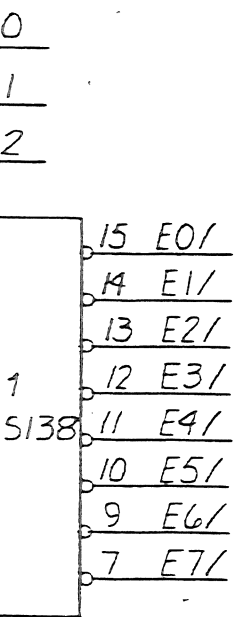
CHIP COMPLEMENT			
QTY	TYPE	+5V	GND
1	74LS00	14	7
4	74LS138	16	8
1	4009	1,16	8
1	4010	1,16	8
3	8T97	16	8
2	8T98	16	8
64	RAM	18	9



\* FOR AMD 9404  
 ADD JUMPERS { A8 TO 14  
                   A9 TO 13  
                   D0 TO 6  
                   D1 TO 7  
                   D4 TO 6  
                   D5 TO 7  
 FOR 2714  
 ADD JUMPERS { A8 TO 6  
                   A9 TO 7  
                   D0 TO 14  
                   D1 TO 13  
                   D4 TO 14  
                   D5 TO 13

DATA	
32K STATIC RAM	
10032	SHT20F2





CONTROL

32 K STATIC RAM	
10032	SHT 10F2