Glitch Works 8085 SBC rev 4 Mini
GW-8085SBC-4M

User's Manual and Assembly Guide

Revision 1, 2024-05-06

http://www.glitchwrks.com/

Contents

1 Introduction

The Glitch Works 8085 SBC rev 4 Mini (GW-8085SBC-4M) is a single-board computer based on the Intel 8085 CPU. It includes the following features:

- Intel 8085 CPU at 3.072 MHz
- 64 KB static RAM, FeRAM compatible
- Up to 512 KB Flash memory in 4K pages, in-board programmable
- Hardware assist bit-bang serial console
- Software controlled power-on jump
- Flash paging and switch-out
- Debounced reset and power supply supervisory circuit
- Glitchbus expansion header

The 8085 SBC rev 4M is a completely self-contained system with a ROM monitor (GWMON-80) and CP/M 2.2. It requires only a serial terminal (or terminal emulation software on a PC) for full operation. The large Flash memory included onboard serves as both the boot ROM and CP/M A: drive.

1.1 GWMON-80 ROM Monitor

GWMON-80 1.1 SM is included with the default Flash software load for the 8085 SBC rev 4M. It supports the following standard commands:

```
D XXXX YYYY     Dump memory from XXXX to YYYY
E XXXX          Edit memory starting at XXXX (CTRL+C to end)
G XXXX          GO starting at address XXXX
I XX            Input from I/O port XX and display as hex
O XX YY         Output to I/O port XX byte YY
L               Load an Intel HEX file into memory
```

An additional `B` command has been added to boot CP/M 2.2 from the Flash chip. Detailed information and source code for GWMON-80 can be found in the Github repository:

`https://github.com/glitchwrks/gwmon-80`

1.2 CP/M 2.2 Features

The default configuration for the 8085 SBC rev 4M includes CP/M 2.2, using the majority of the 512 KB Flash chip as CP/M's `A:` drive. Full 4K Flash sector buffering is implemented, which reduces write wear and amplification, as well as dramatically increasing disk access speed.

In addition to the Flash `A:` drive, the GW-GLITCHBUS-CF1 CompactFlash interface is supported as `B:` drive, with no modification to either the existing CP/M image on the CompactFlash card, or the CBIOS included with the 8085 SBC rev 4M. Simply plugging the CompactFlash interface into the 8085 SBC rev 4M at default addressing (base address of `0x10`) enables the `B:` drive on CompactFlash. CF reads and writes are fully buffered at the 512 byte block level.

The standard software load for the 8085 SBC rev 4M includes `PCGET` and `PCPUT`, allowing XMODEM transfers of files to and from the SBC.

2 Configuration

The 8085 SBC rev 4M uses software configuration for all board options. No switch packs or jumpers need to be set.

2.1 Flash Options

The 8085 SBC rev 4M supports 32-pin Flash chips, ranging in size from 128 KB to 512 KB. The Flash chip is paged into system memory in 4K segments through the ROM segment latch, and can also be disabled entirely. No configuration changes are required to support different Flash sizes; however, all Glitch Works kits ship with 512 KB parts.

Glitch Works parts kits and fully assembled boards use SST 39SF040 Flash chips in DIP-32 packaging. When substituting other manufacturers' parts, ensure that the write and software data protect (SDP) algorithms are the same, and that the chosen part supports 4K sector erase. *Flash chips that require entire device erasure for reprogramming cannot be used as a writable CP/M A: drive!*

2.2 Interrupt Jumpering

The five hardware interrupt lines of the Intel 8085 are pulled down to an inactive state with resistor pack RP1. While they are not used by the default Glitch Works software package, they are available for use. Additionally, the `*BINT` line from the Glitchbus expansion header is inverted and brought to TP1, `INTERRUPT`. It may be jumpered to any of the five available hardware interrupts. Consult the schematic for further details.

2.3 Glitchbus Expansion

The 8085 SBC rev 4M is expandable through a Glitchbus expansion header. The Glitchbus is a generic 8-bit bus intended to be processor-agnostic. Glitchbus expansion cards are designed to stack above or below the SBC using PC/104 style stacking headers. Alternatively, the 8085 SBC rev 4M may be assembled with a right-angle connector for use in backplanes.

Do note that some of the status and control lines are not fully buffered on the 8085 SBC rev 4M and are subject to loading limitations.

All available Glitchbus boards are compatible with the 8085 SBC rev 4M. *The Glitchbus expansion header is not compatible with boards designed for the 8085 SBC rev 1 and 2.* Previous boards are of a different physical size and should be fairly hard to get mixed up with Glitchbus boards.

3 Assembly

The 8085 SBC rev 4M is designed to be easy to assemble for anyone with moderate soldering ability. It is a moderately complex board and will typically require between one and three hours of assembly time, depending on the skill of the assembler. The following tools will be required:

- Soldering iron, 20-40 W recommended, grounded tip
- Solder, 63/37 leaded solder recommended, Kester "44 Core" or similar
- Diagonal cutters or flush cutters
- Solder braid, solder sucker, or desoldering station, in the event errors are made
- Needle-nose pliers for bending component leads
- 1/4 and 1/8 W resistor lead forms (optional)

This manual does not cover basic soldering technique. If you are new to soldering, we recommend the Adafruit soldering guide and plenty of practice on a piece of protoboard, before beginning assembly of the 8085 SBC rev 4M. The Adafruit guide can be found at:

`https://learn.adafruit.com/adafruit-guide-excellent-soldering`

3.1 Assembling the 8085 SBC rev 4M

If you purchased a full Glitch Works parts kit, we recommend completing all assembly sections, since extra features can be disabled as needed. If supplying your own parts, you may choose which sections to complete based on the functionality required.

Note that pin 1 is designated with a square pad for all ICs, resistor packs, switches, and most connectors. Except for the 8085 CPU itself, pin 1 is toward the top of the board, as seen from the front, for all ICs, diodes, resistor packs, and switches. The component (front) side of the board is the side which contains the white silkscreen legend. It is recommended to install components from shortest to tallest, which makes assembly without an assembly vise or jig easier, assuming the board is flipped over and soldered with the component side resting on a table top.

3.2 Assembly Checklist

- ☐ Verify parts list against kit contents or builder-provided parts
- ☐ Consult the assembly drawing for component locations and values
- ☐ Bend all 0.1 µF bypass capacitors (axial bead) – position 2 on a 1/8 W lead form
- ☐ Install all 0.1 µF capacitors in positions marked C in assembly diagram
- ☐ Bend 4.7 kΩ resistors and install in their marked locations – position 1 on a 1/4 W lead form
- ☐ Bend all 330 Ω resistors and install in their marked locations – position 1 on a 1/4 W lead form
- ☐ Install non-socketed DIP ICs at their marked locations. Do not install U2, U5, or U10
- ☐ Install a 40-pin socket at U2
- ☐ Install a 32-pin socket at U5
- ☐ Install a 24-pin narrow DIP socket at U10
- ☐ Install 22 µF 10V capacitor at C13, bend leads with needle-node pliers
- ☐ Install 10 nF radial ceramic capacitor at C1
- ☐ Install resistor pack at RP1
- ☐ Install TO-92 DS1233 at U1
- ☐ Install two six-pin headers for serial mezzanine at A1
- ☐ Install three LEDs at D1, D2, D3
- ☐ Install 6.144 MHz CPU clock crystal at Y1

3.3 Insert Socketed ICs

- ☐ Insert 8085 CPU into socket at U2
- ☐ Insert 39SF040 EEPROM (`8085R4-M CP/M 2.2` on label) into socket at U5
- ☐ Insert 22V10 GAL (`85R4M` on label) into socket at U10

3.4 Right Angle or Stacking Configuration

The 8085 SBC rev 4 Mini can be expanded using stacking Glitchbus modules, or a Glitchbus backplane. The intended configuration will determine which connector should be used.

When using the right-angle connector option, *install the connector on the solder side of the board* to maintain correct spacing to the backplane card guides, and to ensure electrical compatibility with stacking connectors. A Glitchbus board with a right-angle connector installed on the solder side may be plugged directly into a stacking connector.

The 8085 SBC rev 4M can be populated with either straight or right-angle reset button and power header options. The reset button footprint is a dual part footprint and will work with either button

type. The power header is spaced such that the block of the right angle header will be at the board edge.

- ☐ Install micro tact pushbutton at SW1
- ☐ Install power header at J1
- ☐ Install Glitchbus expansion connector at J2

3.5 Connect Serial Mezzanine

The 8085 SBC rev 4M uses a serial mezzanine to convert TTL `TX` and `RX` signals into the desired interface. It is compatible with Glitch Works mezzanines, as well as "FTDI cable" USB adapters. If using a USB adapter, be sure that its pinout matches the signals on the A1 connector before use.

The onboard system serial console does not support hardware handshake. If your terminal requires hardware handshake, ensure that your cabling satisfies its signal requirements. A serial light box will help debug potential serial wiring problems. We highly recommend the addition of a light box to your toolkit if you regularly interface RS-232 equipment, our personal favorite is the IQ Technologies SmartCable SC821 Plus.

3.6 Power Supply Considerations

The 8085 SBC rev 4M may be powered by either the 5V power connector (J1), or through the serial mezzanine connector, *but not both at once*. When using a "FTDI cable" style USB adapter, small systems may be powered from USB alone.

When used with Glitchbus expansion cards, the 8085 SBC rev 4M may receive power from the Glitchbus, or provide power to other cards through the Glitchbus. The 8085 SBC rev 4M may be used to power other Glitchbus cards through the serial mezzanine connector in either configuration.

Any external power supply should provide 5 V and at least 500 mA. 5 V rail regulation should be within 5% – outside of this range, the DS1233 EconoReset will hold the system in reset, preventing operation.

4 Initial Checkout and Testing

Once the 8085 SBC rev 4M is assembled, double-check all ICs for proper orientation, and check all solder joints for cold joints or solder bridges. Connect the power pigtail provided to a suitable regulated 5 V power supply capable of providing at least 500 mA, or use USB power. Connect your serial terminal or computer to the console port. Apply power to your system and press `RESET`. The GWMON-80 sign-on message should be printed to the console, and GWMON-80 should respond to appropriate user input. `POWER ON` and `ROM ON` LEDs D1 and D2 should be lit. `ROM BOOT` should flash briefly during reset.

After confirming operation with GWMON-80, press `B` at the GWMON prompt to boot into CP/M 2.2. CP/M will respond with the `A>` prompt. Included on the default Flash chip load is the Rasmussen memory test program, called `MEMR.COM` in the CP/M file system. We recommend running `MEMR` and allowing it to complete several passes as part of the initial checkout process. This will take 10-15 minutes.

4.1 Troubleshooting

If your 8085 SBC rev 4M fails to come up, recheck all solder joints for cold joints, bridges, or missed pins – this is by far the most common problem we've observed during assembly workshops. Ensure your serial terminal or terminal emulator software is properly configured and that your cable is wired correctly (a RS-232 light box is very helpful here).

Verify that `*BRESET` is properly strobing during power-up and when pressing the `RESET` button (SW1). If the `ROM ON` (D2) LED does not light after reset, or the `ROM BOOT` LED does not flash, the fault is likely in either the boot flop-flop or ROM segment latch.

4.2 Repair and Service

If you purchased an assembled 8085 SBC rev 4M from Glitch Works, LLC, your board is warranted to work on arrival. If you have assembled a kit that fails to work, you may return it to Glitch Works, LLC for evaluation, repair, and testing. For questions concerning returns or configuration, please visit `http://www.glitchwrks.com/` and click the "Contact" link.

Do note that while we will attempt to help those who have purchased used boards, there is no warranty extended.

5 Technical Notes

5.1 ROM Segment Latch

The 8085 SBC rev 4M includes a ROM segment latch, which is implemented as an 8-bit latch with readback at I/O address `0xFF`. This latch controls which 4K segment of the Flash chip is active, and whether the Flash chip is enabled or disabled. It is cleared to `0x00` on reset. The bits of the ROM segment latch are mapped as follows:

Register Bit	Function	Notes
7	ROM Enabled	Cleared (LED off, ROM disabled) on reset
6	ROM Segment Address, bit 6	Cleared on reset
5	ROM Segment Address, bit 5	Cleared on reset
4	ROM Segment Address, bit 4	Cleared on reset
3	ROM Segment Address, bit 3	Cleared on reset
2	ROM Segment Address, bit 2	Cleared on reset
1	ROM Segment Address, bit 1	Cleared on reset
0	ROM Segment Address, bit 0	Cleared on reset

Bits 0-6 control the selected 4K segment of Flash available at `0xF000 - 0xFFFF`. These bits are cleared on reset so that the first segment of ROM is available for booting. Writing to these bits immediately changes the ROM segment.

Bit 7 enables Flash when set, and disables Flash when cleared. This allows unmapping Flash for use of the full 64 KB of system memory. Writing a `0` to this bit clears it and immediately switches off Flash, writing a `1` to this bit switches Flash in. The selected Flash page is not affected if no other bits are modified. The reset state of bit 7 is `0`.

The ROM segment latch is implemented as an 8-bit latch with readback. Reading from I/O port `0xFF` returns its current value.

5.2 Default Memory Map

Address Range	Contents
`0x0000 - 0x7FFF`	Static RAM, IC socket U15
`0x8000 - 0xEFFF`	Static RAM, IC socket U16
`0xF000 - 0xFFFF`	Static RAM, IC socket U16, when Flash is disabled
`0xF000 - 0xFFFF`	4K page of Flash, IC socket U19, when Flash is enabled

Onboard memory devices may be overlaid by external devices on the Glitchbus using the `*BMASK` signal.

5.3 Default I/O Map

I/O Address	R/W	Function
`0xFF`	R/W	ROM Segment Latch

Note that the ROM segment latch is implemented with readback. The hardware assist bit-bang serial console occupies no I/O space.

6 Parts List

The following substitutions may be made if you have purchased a bare board and are supplying your own parts, or in a full Glitch Works parts kit:

- Any compatible 7400 series family logic ICs may be used (for example, a 74LS04 in the parts list may be shipped as a 7404, 74S04, 74F04, 74LS04, 74ALS04, or 74HCT04).
- All 4.7 kΩ resistors on the 8085 SBC rev 4M are pull-up or pull-down resistors, and may be any value from 2.2 kΩ to 10 kΩ, even though they are indicated as 4.7 kΩ on the assembly drawing
- Resistors may be of varying precision and body type

If you purchased a full Glitch Works parts kit, be sure it includes the following:

☐ 11x axial bead ceramic capacitor

☐ 1x 10 nF 16 V radial ceramic capacitor

☐ 1x 22 µF 10 V axial tantalum capacitor

☐ 3x 330 Ω 1/4 W resistor

☐ 5x 4.7 kΩ 1/4 W resistor (see above note)

☐ 1x 4.7 kΩ x 5 SIP resistor pack (see note above)

☐ 1x 6.144 MHz crystal

☐ 1x 8085 CPU

☐ 1x 39SF040 512K x 8 Flash chip, preloaded with GWMON-80 and CP/M 2.2

☐ 2x JEDEC 62256-type 32K x 8 static RAM

☐ 1x 22V10-type GAL, preloaded with default configuration

☐ 2x 74LS245 transceiver

☐ 1x 74LS373 octal D-type latch

☐ 1x DS1233 EconoReset

☐ 3x red T-5 LED

☐ 1x mini tact pushbutton switch

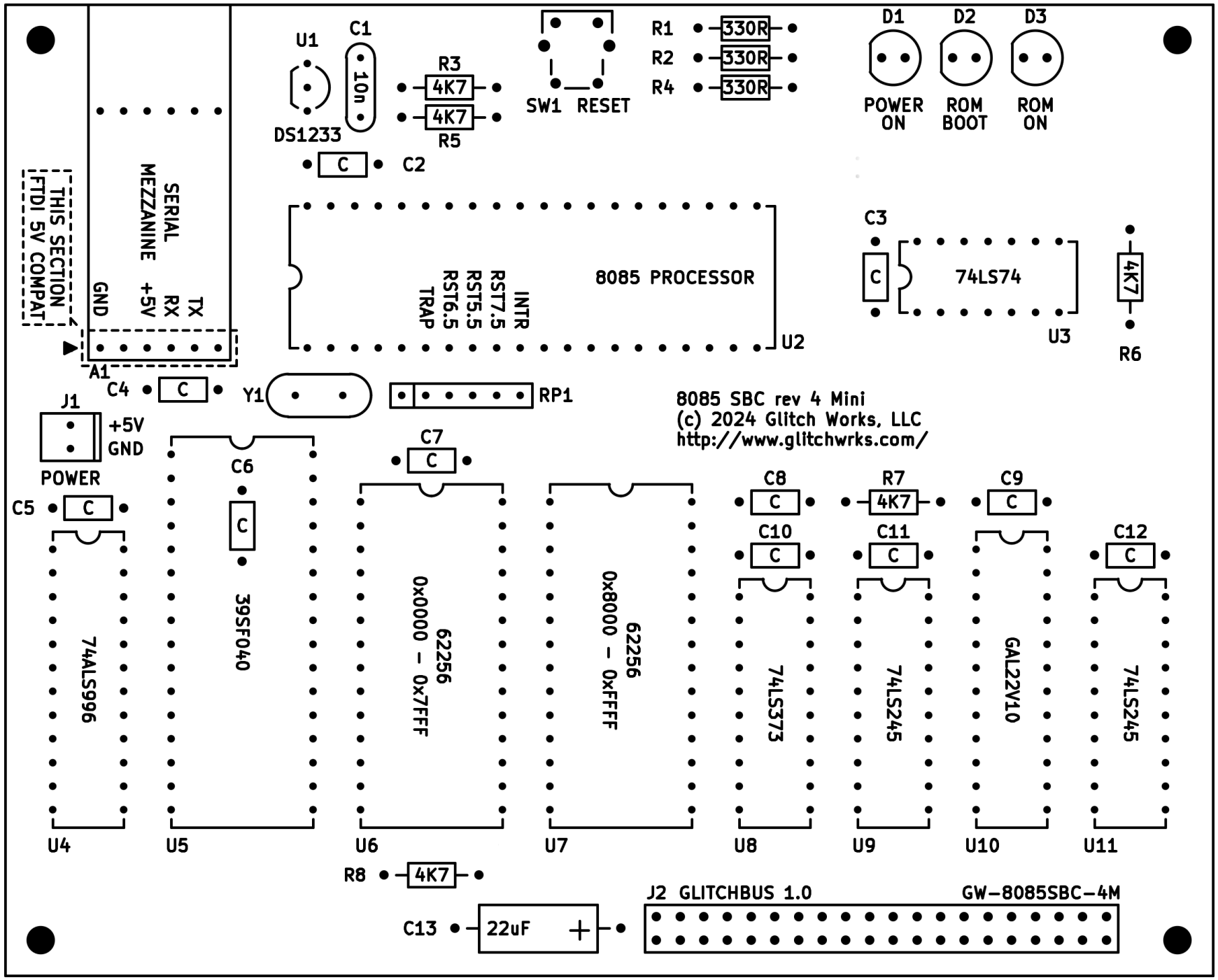
☐ 2x 6-pin header strip

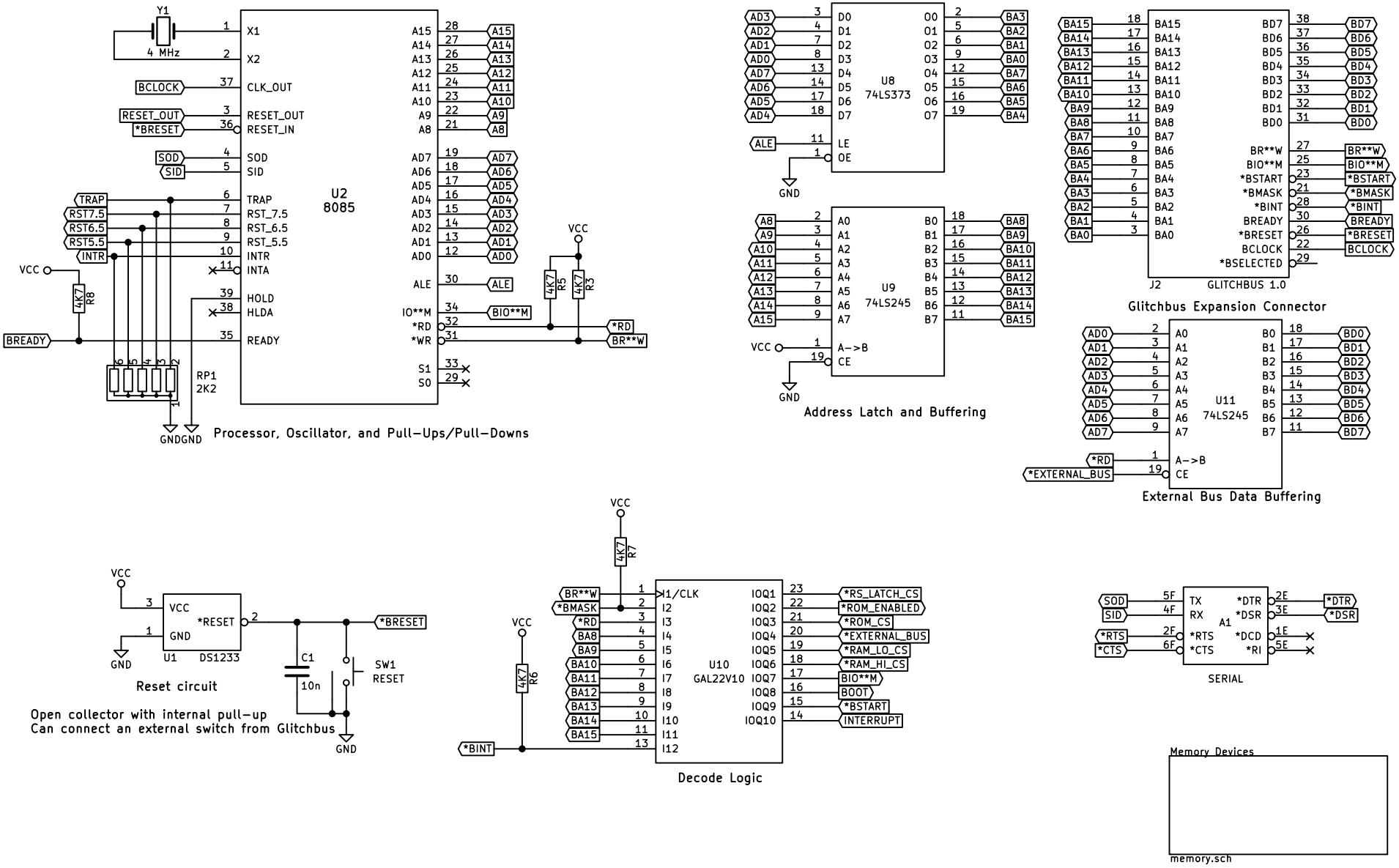
☐ 1x 2-position Molex KK-100 header

☐ 1x 40-pin IC socket

☐ 1x 32-pin IC socket

☐ 1x 24-pin narrow IC socket


U1
C1
10n
DS1233
R3
4K7
4K7
R5
C
C2
SW1
RESET
R1
330R
R2
330R
R4
330R
D1
D2
D3
POWER ON
ROM BOOT
ROM ON
THIS SECTION FTDI 5V COMPAT
SERIAL MEZZANINE
GND
+5V
RX
TX
A1
8085 PROCESSOR
TRAP
RST6.5
RST5.5
RST7.5
INTR
U2
C3
C
74LS74
U3
4K7
R6
C4
C
Y1
RP1
8085 SBC rev 4 Mini
(c) 2024 Glitch Works, LLC
http://www.glitchwrks.com/
J1
+5V
GND
POWER
C5
C
C6
C
C7
C
C8
C
C10
C
R7
4K7
C11
C
C9
C
C12
C
74ALS996
39SF040
62256
0x0000 – 0x7FFF
62256
0x8000 – 0xFFFF
74LS373
74LS245
GAL22V10
74LS245
U4
U5
U6
U7
U8
U9
U10
U11
R8
4K7
C13
22uF
J2 GLITCHBUS 1.0
GW-8085SBC-4M



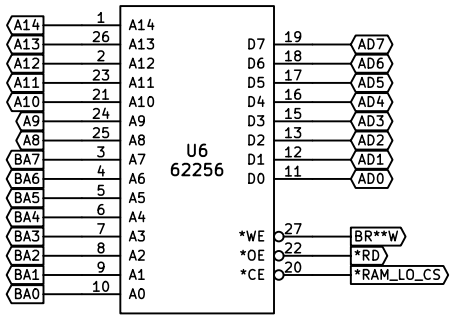
CPU, Glitchbus Interface, and Control

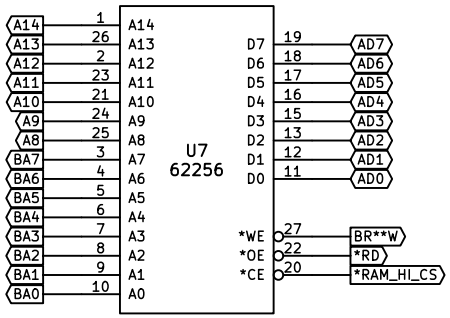
J. Chapman
Glitch Works, LLC

Sheet: /
File: gw-8085sbc-4m.sch

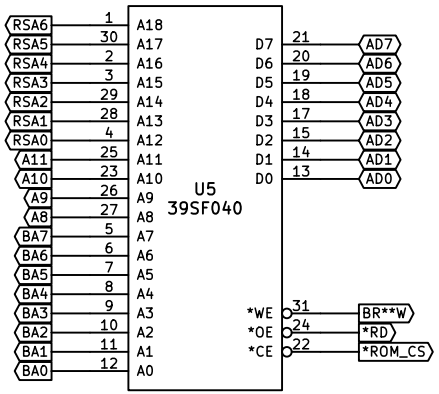
Title: 8085 SBC rev 4 Mini

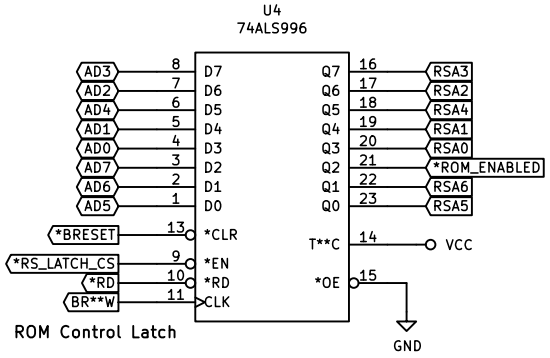
Size: USLetter	Date: 2024-03-07	**Rev: PRODUCTION**
KiCad E.D.A. kicad 5.1.2		Id: 1/2





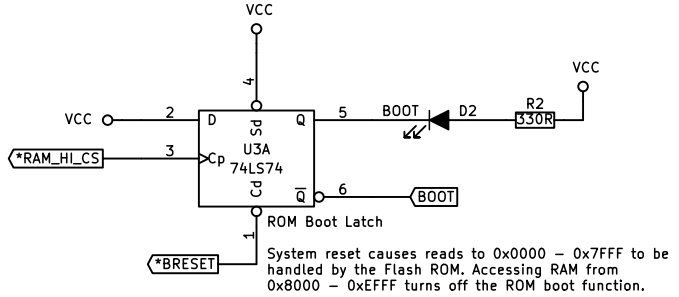
Memory Devices





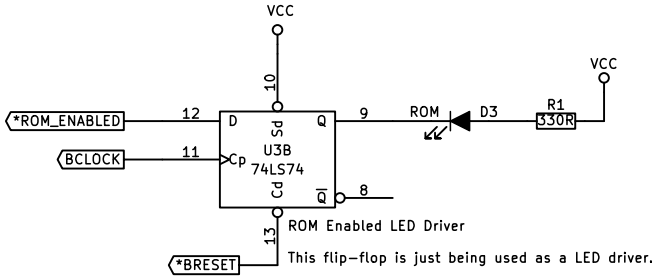
ROM Control Latch

This latch controls which 4K segment of ROM is addressed.
Cleared to 0 on *RESET, writable at IO_BASE + 2
Bits 0 – 6 set ROM page, bit 7 disables ROM when set to 1.



ROM Boot Latch

System reset causes reads to 0x0000 – 0x7FFF to be handled by the Flash ROM. Accessing RAM from 0x8000 – 0xEFFF turns off the ROM boot function.



ROM Enabled LED Driver

This flip-flop is just being used as a LED driver.

Memory Devices, ROM Segment Control, Boot Control		
J. Chapman **Glitch Works, LLC**		
Sheet: /Memory Devices/ File: memory.sch		
Title: 8085 SBC rev 4 Mini		
Size: USLetter	Date: 2024-03-07	**Rev: PRODUCTION**
KiCad E.D.A. kicad 5.1.2		Id: 2/2

```
GAL22V10        ; 8085 SBC rev 4 Decode Logic
8085SBC4        ; PRODUCTION 1


;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;Pin Declarations
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
BRW
BMASK
RD
BA8
BA9
BA10
BA11
BA12
BA13
BA14
BA15
GND

BINT
INTRPT
BSTART
BOOT
BIOM
RAMHICS
RAMLOCS
EXTBUS
ROMCS
ROMENA
RSLATCS
VCC

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;Equations
;
;Low RAM 0x0000 - 0x7FFF when BOOT is low, disabled when
;BOOT is high
;
;High RAM controlled as follows:
;       * 0x8000 - 0xBFFF when BOOT is high
;       * 0x8000 - 0xEFFF when BOOT is low, ROMENA is low
;       * 0x8000 - 0xFFFF when BOOT is low, ROMENA is high
;
;Flash ROM controlled as follows:
;       * All memory locations when BOOT is high
;       * 0xF000 - 0xFFFF when BOOT is low and ROMENA is low
;       * Disabled when BOOT is low and ROMENA is high
```

```
;
;ROM segment latch at I/O address 0xFF R/W
;
;EXTBUS output is low when no onboard memory or I/O devices
;are addressed.
;
;BMASK low inhibits any onboard memory.
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
BSTART          =       RD * BRW

INTRPT          =       /BINT

/RSLATCS        =       BA15 * BA14 * BA13 * BA12 * BA11 * BA10 * BA9 * BA8 * BIOM

/ROMCS          =       BOOT * /BIOM
                        + BA15 * BA14 * BA13 * BA12 * /BIOM * /ROMENA * BMASK

/RAMLOCS        =       /BA15 * /BIOM * /BOOT * BMASK

/RAMHICS        =       BA15 * /BIOM * ROMCS * /BOOT * BMASK
                        + BA15 * /BA14 * /BIOM * BOOT

/EXTBUS         =       RSLATCS * ROMCS * RAMHICS * RAMLOCS

;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;Notes
;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
DESCRIPTION

This PALASM file describes the logic used on the Glitch Works 8085
SBC rev 4 Mini.
```